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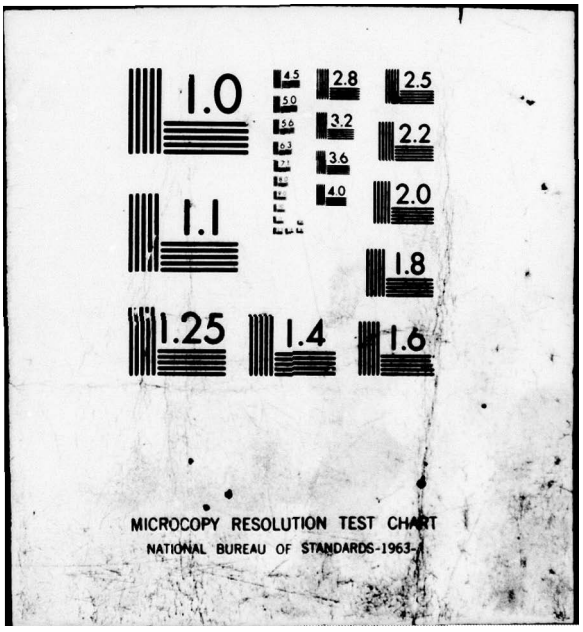
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FINAL REPORT

TRANSIENT–THERMAL BEHAVIOR OF PULSED HIGH POWER IMPATT AND TRAPATT DIODES

by
John W. Amoss

Prepared for
U. S. ARMY RESEARCH OFFICE
Grant No. DAAG29–76–C–0202

12 JUNE 1979

GEORGIA INSTITUTE OF TECHNOLOGY
Engineering Experiment Station
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Results of an analytical investigation of transient and steady state temperature and current profiles within the active region of a variety of IMPATT structures are presented. The analyses are based on thermal models which assume power dissipation distributions with an axial dependence proportional to the electric field intensity E(z) and a radial dependence proportional to the local

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current density j(r). Examples are presented in which the local current density is assumed to decrease with the local temperature, according to the expression $j(r) = a[V-V_0-b(T-T(r))]$.

The temperature gradients within the active region depend strongly on the doping profile. These analyses show that the maximum temperature at the edge of the active region can be as much as 25% higher than at the center of the avalanche region, especially for high efficiency, high power structures where the ionization is highly localized and the electric field intensity in the drift region is sufficiently high to prevent unsaturated drift velocities and depletion-layer modulation. Breakdown calculations using temperature dependent ionization coefficients and axial temperature profiles suggest that actual temperatures within a device can be significantly higher than those measured experimentally by using a predetermined breakdown voltage vs temperature calibration curve.

Curves are presented which show normalized current density and axial and radial temperature profiles within the active region of selected devices for various values of time.

Quasi-empirical small-signal models of lo-hi-lo structures based on curve fitting experimental data are presented. Low-frequency instabilities of IMPATT chips connected in series are discussed in terms of the device's complex natural resonant frequency.

TRANSIENT-THERMAL BEHAVIOR OF PULSED HIGH POWER IMPATT AND TRAPATT DIODES

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PREFACE

The work described herein was performed in the Solid State Sciences Division of the Applied Sciences Laboratory, Engineering Experiment Station, Georgia Institute of Technology under U. S. Army Research Office Grant No. DAAG29-76-C-0202. Principal Georgia Tech Contributors were J. W. Amoss, T. B. Elfe, and S. A. Lubs (Student).

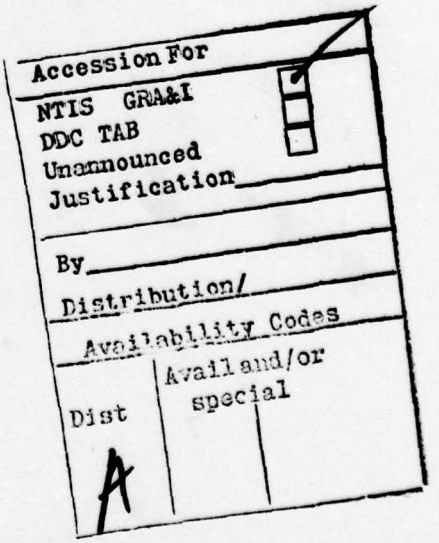

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

LIST OF TABLES

SECTION I

INTRODUCTION

PROBLEM STATEMENT

During the past years, much effort has been devoted towards increasing the output power capabilities of microwave solid state devices. These efforts, especially in the area of active d.c. to microwave sources, have mainly concentrated on increasing output power by (1) improving the electrical and thermal properties of individual semiconductor chips, (2) combining the output power of several semiconductor chips at the chip level, or (3) combining the output power of several prepackaged semiconductor chips at the circuit level. The first two efforts have led to rather complicated devices. The problems of characterizing their electrical and thermal properties have become more and more difficult as their complexity increased.

OBJECTIVES

The primary objective of this program was to develop useful models with which the transient-thermal properties of high-power IMPATT devices could be evaluated. Although the thermal analysis and device characterization techniques were to be applicable to the modeling of other high-power semiconductor devices, IMPATTs were chosen for this study because of the very high-power and correspondingly high temperatures at which they operate. High-power IMPATTs are probably stressed as close to the constituent materials maximum temperature limits as any other microwave semiconductor device. Because of this, their operating characteristics are more temperature dependent than that of other devices.

The tasks of the program were aimed at developing analytical models or numerical capabilities which could be used to characterize the transient thermal and electrical properties of high-power IMPATTs. Specifically they were:

- to determine the transient-thermal properties of the various structures and mounting geometries currently used in high-power IMPATTs,
- to identify and determine the temperature-dependent material and physical parameters, and
- to investigate the effects of temperature cycling on the overall characteristics of pulsed IMPATT oscillators.

SUMMARY OF WORK

The thermal analysis program used in this study, the Martin Interactive Thermal Analysis System - Version II (hereafter referred to as MITAS-II), proved to be a versatile and powerful (although, in some cases, expensive) diagnostic tool for obtaining two and three dimensional steady-state and transient temperature distributions within the active region of complex high-power IMPATTs. Heretofore, the thermal analyses of these devices had been restricted to one dimensional heat source models. MITAS II is capable of handling 8191 node problems with reasonable efficiency and, thus, of providing a detailed analysis of the temperature distributions within rather complicated structures. The computer program was readily adaptable to semiconductor devices and allowed both steady-state and transient analyses to be made under the following conditions:

- temperature-dependent thermal conductivity and specific heat,
- nonuniform power dissipation in active region, and
- materials and metallizations of finite volumes and dissimilar shapes between active region and assumed isothermal boundaries.

Representative transient and steady-state temperature and current profiles within the active region of hi-lo IMPATT structures of gold plated heat sink (PHS) construction are presented in Section II. The power dissipation distributions used in the thermal analyses assumed an axial dependence proportional to the electric field intensity and a radial dependence proportional to the local current density. These were determined from d.c. breakdown calculations.

In general, the CW or high-duty cycle pulsed thermal characteristics of these devices are greatly improved when mounted on diamond. For low-duty cycle pulsed operation where the average dissipated power is low, the improvement realized in mounting a PHS device on a diamond vs another material depends upon the pulse length and the thickness of the PHS. These calculations show that when $\tau \leq H^2/\alpha$ (where H is the thickness, α the diffusivity of the PHS material and τ the pulse length) no significant advantage is realized in the diamond mounting for low duty cycle operation.

Similar calculations of multichip devices with center-to-center spacings of $4r_o$ (where r_o is the radius of the chips) showed no mutual heating for low-duty cycle operation and pulse widths less than about 10 microseconds. For high duty-cycle or CW operation, however, mutual heating effects will occur and should be taken into account when determining an overall thermal resistance for a multichip array.

The temperature at the substrate edge of the depletion width of a highly-efficient hi-lo structure was found to be significantly higher than at the center of the avalanche region. One should allow for these temperature gradients when using a measured "device temperature" to interpret temperature related phenomena effecting reliability such as solder "creep",

thermal stresses, etc. A breakdown voltage vs temperature curve, usually predetermined under isothermal conditions, is normally used in making such measurements. The device temperature thus obtained will invariably be the average temperature of the avalanche region. The temperature profile within the active region and, hence, the temperature of other points relative to the "measured temperature" can be approximated for devices of known doping by the methods outlined in Section II.

The structural and material parameters must be accurately known to obtain quantitative agreement between calculated and measured operating characteristics of hi-lo and lo-hi-lo devices. At present, there is considerable uncertainty in the ionization rates and drift velocities for GaAs at the high field levels where these devices operate. Admittance calculations based on generalized small-signal theory could not be brought into agreement with the measured admittance of lo-hi-lo devices. Whether this was due to uncertainties in the material and structural parameters or to effects not included in the theory could not be determined unambiguously because of the many parameters involved in the numerical solution. An approximate analytical model is given in Section III which closely approximates admittance calculations obtained by more exact methods. The analytical model contains two elements which can be adjusted to simulate effects not easily included in the more generalized theory, such as tunneling and/or diffusion.

The breakdown calculations described in Section IV utilizes the pseudo-local approximations of Okuto and Crowell[28] to determine temperature dependent effective ionization rates from experimental data. The rates thus obtained are in reasonable agreement with values extrapolated from the low-field

measurements recently reported by Pearsall, et al.[32]

The effective ionization rates were used to calculate certain device parameters. Others were obtained by curve fitting experimental data. Current multiplication factors of about 100 were required to fit the experimental data for devices with avalanche widths of about 2500 Å. For devices with thinner avalanche widths, the multiplication factors were considerably lower. The temperature dependency of these effects could not be accurately modeled.

Interpreting the experimental data in terms of a complex natural resonant frequency helped resolve the cause of severe stability problems encountered on a chip level power combining program conducted concurrently here at Georgia Tech. The comparative stability of series connected lo-hi-lo GaAs chips and uniformally doped Si chips are discussed at the conclusion of Section IV.

SECTION II

THERMAL ANALYSES

INTRODUCTION

The characteristics of IMPATT oscillators and amplifiers are greatly influenced by the thermal properties of the mounted diode. On one extreme, catastrophic failure or burnout results due to a thermal runaway process[1-3] if the temperature of the material exceeds a certain value. Consequently, the power dissipated within an IMPATT device and, hence, the r.f. power delivered to a useful load for a given conversion efficiency are often limited by the maximum temperature the semiconductor material is allowed to reach. Even if the temperature of the material is kept below the burn-out value, continuous operation at elevated temperatures causes subtle changes in the performance, reliability, and useful life of the device. These long term changes are due to solder and ion migration, thermal-mechanical stress, and other temperature related phenomena which gradually degrade overall performance. On the other extreme, transient temperature gradients which occur within the active region of a pulsed device, even when operated at low power levels, cause leading edge jitter, spectral breakup, and a.m. and f.m. modulation within the pulse.[4]

Because thermal effects are of such importance in the operation of IMPATT devices, a number of investigations on this subject have been reported by others in the past. The majority of these, however, reported results based on steady-state or transient analyses of idealized thermal models which assumed heat sources of zero thickness. For example, Haitz,[4] in pointing out the origin of nonuniform current density and its effect on device performance, modeled the heat source as a disk of zero thickness

located at the surface of the semiconductor. Gibbons and Misawa,[5] in comparing junction temperature and current profiles of circular devices with that of ring devices, used similar models. Holway[6] more recently developed a dimensionless model which allows the temperature and current density to be approximated across a circular device. His model is also based on a heat source of zero thickness and like [5] assumes the heat source to be located on the surface of a semi-infinite heat sink. A number of transient analyses have also been reported by others. Few of these, however, considered the heat source to be of finite volume. One recent exception is Olson[7] who reported the results of a one-dimensional analysis which gave the transient temperature response at selected points along the axis of uniformly doped devices.

The thermal calculations made during the first phase of this program augment those reported by Olson[7] and others.[4,5,6] A two dimensional heat flux model was used to calculate the axial and radial transient temperature profiles and the transient current density within the active region of a variety of IMPATT devices mounted on composite heat sinks.

The analyses were performed using a general purpose thermal computer program developed originally to analyze heat flow for aerospace applications.* The computer program, readily adaptable to semiconductor devices, allowed both steady state and transient analyses to be made under the following conditions:

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* Called MITAS II, the computer program was developed by Martin, Marietta Denver Division and evolved from a program entitled CINDA-3G, developed by Chrysler Corporation Space Division at NASA's Michoud Assembly Facility. A brief description of the program is given in Appendix A.

- temperature dependent thermal conductivity and specific heat,
- nonuniform power dissipated in active regions,
- finite materials and metallizations between active region and heat sink, and
- composite heat paths of dissimilar shape and of finite size.

Figure 1 shows thermal conductivity and thermal capacity per unit volume (mass density times specific heat) as a function of temperature for the significant materials used in the construction of the devices analyzed. The computer program required "look up" tables which were based on these curves and were used during each iteration. The dissipated power distributions were obtained from the calculated electric field intensity and current density as discussed in Section IV. For the case where the current density was assumed to vary with temperature, the dissipated power distributions were also adjusted during each iteration.

THERMAL MODEL

The basic device was modeled as a GaAs Schottky junction of gold plated heat sink (PHS) construction. The PHS side (junction side) of the device is t.c. bonded to a diamond chip mounted on a copper slug. Top contact is made to the substrate side via a pair of crossed gold wires. The geometry assumed for the computer model is shown in Figure 2. The semiconductor material, the plated heat sink, and the diamond chip are assumed to be circularly symmetric about the center line of a mesa junction. Although the shape of the PHS and diamond chip are usually rectangular in practice, it was found that computational time was greatly reduced with little change in accuracy by considering those regions to be cylindrical in shape. Similarly, increasing the radial dimensions of the PHS and the diamond also had little effect on the temperature distributions within the

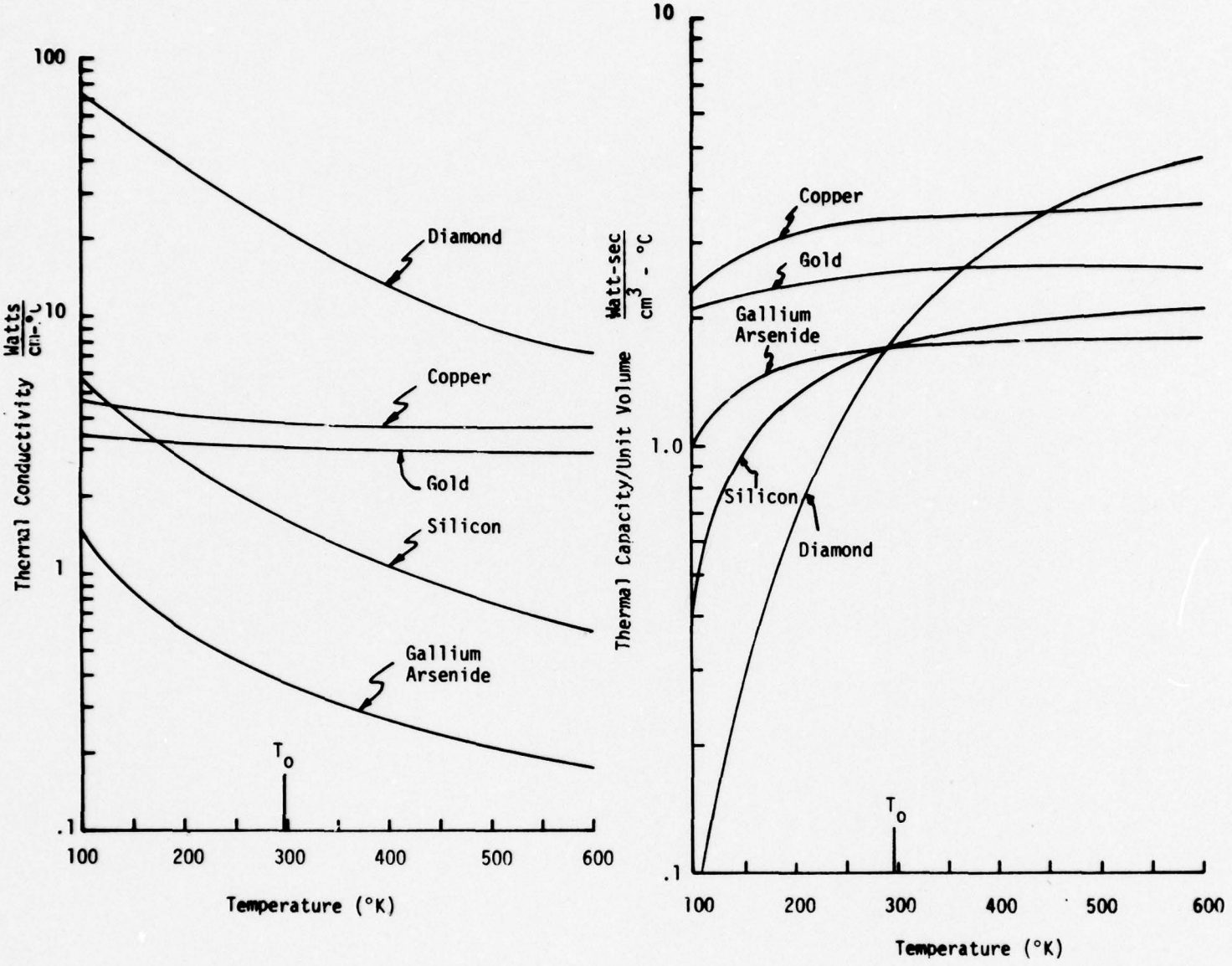


Figure 1. Thermal Conductivity and Thermal Capacity per Unit Volume vs Temperature for Selected Materials.

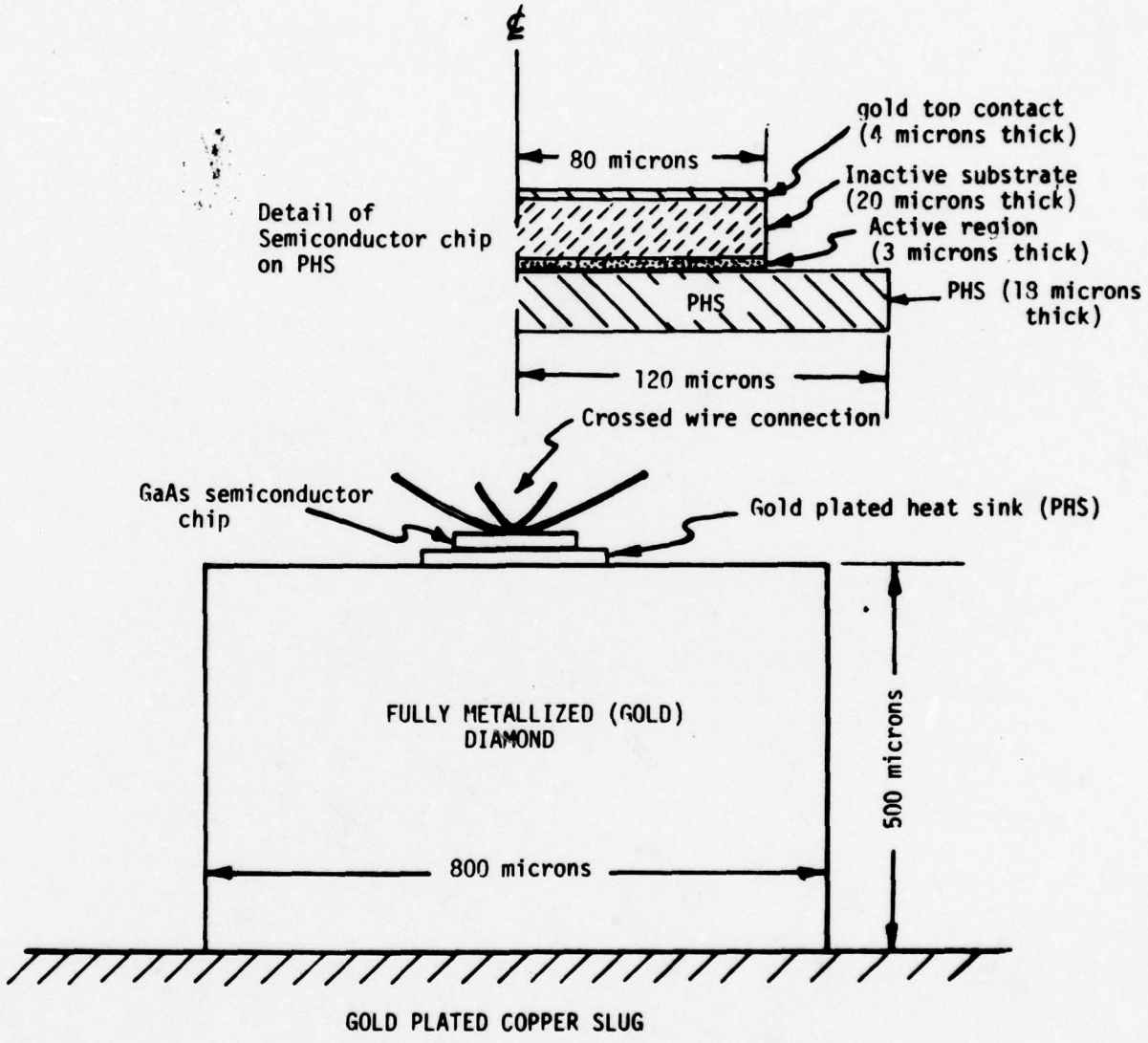


Figure 2. Thermal Model of IMPATT Device.

active region of the various devices. The other end of the top contact wires and the copper slug on which the diamond is mounted are assumed to be maintained at ambient temperature (22 °C).

STRUCTURES ANALYZED

The various IMPATT structures analyzed on this program were classified in terms of semiconductor material, junction type, and doping profile. They were further classified as to geometry, i.e., single mesa or multimesa devices.

Most of the structures analyzed were of single mesa circular geometry, constructed of either Si or GaAs material. Of these, the majority were GaAs devices with either low-high-low or high-low doping profiles. Two basic junction types were considered - diffused (or grown) and Schottky. The thermal models for the two differed mainly in that the diffused junction model contained an extra layer of semiconductor material between the active region and the heat sink approximately 1.5 microns thick.

Heavy emphasis was placed on GaAs Schottky structures, since single chip devices made of this material are now capable of producing several watts at frequencies as high as 10 GHz with efficiencies above 20%.[8-9] There remain problems with GaAs high efficiency devices, particularly in terms of excess noise, gradual degradation in performance and reliability, and premature burnout. These problems are, in part, caused by thermal effects.

Specific single mesa structures which were analyzed are listed in Table I.

TABLE I

DEVICE STRUCTURES

Structure No.	Type of Material	Type of Junction	Doping Profile	Distribution of Heat Flux Added in Depletion Region
I	Si	Diffused	Uniform	f(z)
I′	Si	Diffused	Uniform	f(r,z)
II	GaAs	Diffused	Uniform	f(z)
II′	GaAs	Diffused	Uniform	f(r,z)
III	GaAs	Schottky	Uniform	f(z)
III′	GaAs	Schottky	Uniform	f(r,z)
IV	GaAs	Schottky	lo-hi-lo	f(z)
IV′	GaAs	Schottky	lo-hi-lo	f(r,z)
Va,b,c,d	GaAs	Schottky	hi-lo	f(z)
V′a,b,c,d	GaAs	Schottky	hi-lo	f(r,z)

The remainder of this section will present and discuss typical transient and steady-state temperature and current profiles obtained with structures III and V. Results for the latter are also typical of those for the lo-hi-lo structure.

The overall geometry and dimensions of the devices remained fixed throughout the calculations. Their doping profiles were varied to similate different Schottky uniformly doped and hi-lo doped n-type IMPATTs.* The thickness of the more highly doped region was varied from 0.2 microns to 3.0 microns with the total depletion width kept at 3.0 microns in all cases. By also varying the doping density, a wide range of lo-hi structures were

* The junctions were assumed to be located at the PHS-semiconductor interface and the breakdown conditions were determined as if they were one-sided abrupt p-n junctions[11].

simulated having different dissipated power distributions within the active region. The doping profiles of those reported on here, Table II, are based on similar ones chosen by Schroeder and Haddad[10] for efficiency analyses. Calculated maximum efficiency for these devices range from about 12% for Vd to about 25% for Vb.

TABLE II

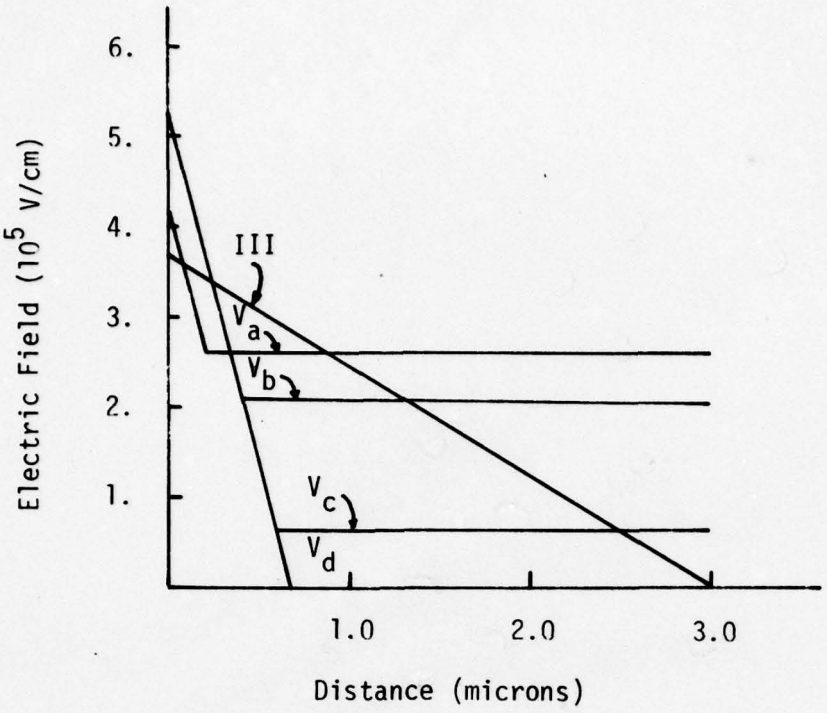
DEVICE DOPING PROFILES

Device Number	N_1 (cm^{-3})	X_1 (microns)	N_2 (cm^{-3})	X_a (microns)
III	8×10^{15}	3.0	--	0.89
Va	5×10^{16}	0.2	1×10^{14}	2.78
Vb	5×10^{16}	0.4	1×10^{14}	0.37
Vc	5×10^{16}	0.6	1×10^{14}	0.26
Vd	5×10^{16}	0.8	1×10^{14}	0.26

NUMERICAL RESULTS AND DISCUSSIONS

The parameters used in the thermal computer program to model the dissipated power distributions were obtained theoretically from static breakdown calculations using the breakdown equations given by Sze[11] and the temperature dependent equal ionization rates given by Hall and Leck.[12] The calculated electric field intensity and generated particle current distributions are shown in Figure 3 for the doping profiles given in Table II. The avalanche widths were taken to be the distance over which 95% of the total particle current was generated.

The dissipated power density used in the computer program was assumed to be equal to the product of the calculated electric field intensity and



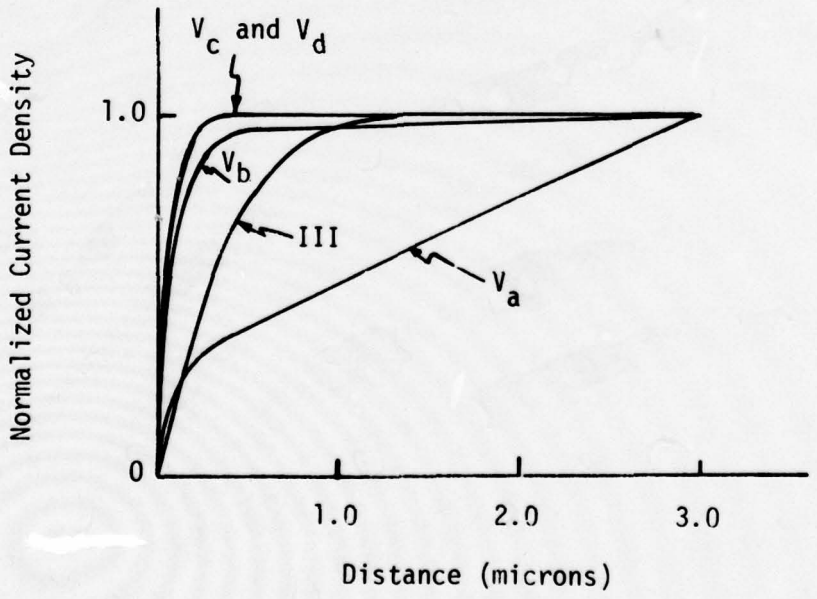


Figure 3. Computed Electric Field Intensity and Normalized Electron Current Density for Uniformly Doped and High-Low Doped GaAs Devices.

an assumed current density. This was incorporated into the computer program by requiring the dissipated power to have an axial dependence proportional to the normalized electric field intensity and a radial dependence proportional to an assumed current density. The current density j(r) was assumed to decrease linearly with the local temperature according to the expression $j(r) = a(V-V_0-b(T(r)-T_0)$ where a is the space charge conductance per unit area, V and V_0 are the operating voltage and breakdown voltage at the heat sink temperature T_0, b is the temperature coefficient of breakdown voltage, and T(r) is the average local temperature within the avalanche zone at the radial distance r from the center line. For example, the uniformly doped device results in a punch-through factor of 1.0 at ambient temperature, a breakdown voltage of 57.0 volts, a temperature coefficient of .10 volts/C, and a space charge conductance per unit area of 380 mhos/cm^2. The latter was calculated from the expression

$$a = 2\varepsilon v(w-x_a)^2$$

where $\varepsilon = 12\ \varepsilon_a$ f/cm,

$v = 8 \times 10^6$ cm/sec, and

$x_a = .89$ microns.

The transient temperature at various points within the uniformly doped device is shown in Figure 4 and 5 for a constant power step of 20.9 watts (5.0 cal—sec^{-1}). The curves of Figure 4 are similar to those for the X-band GaAs device mounted on diamond reported by Olson, except here the heat flux added is assumed to be proportional to local current density as discussed previously. The hottest point originates at the junction center, but quickly moves away from the heat sink. As the temperatures stabilize,

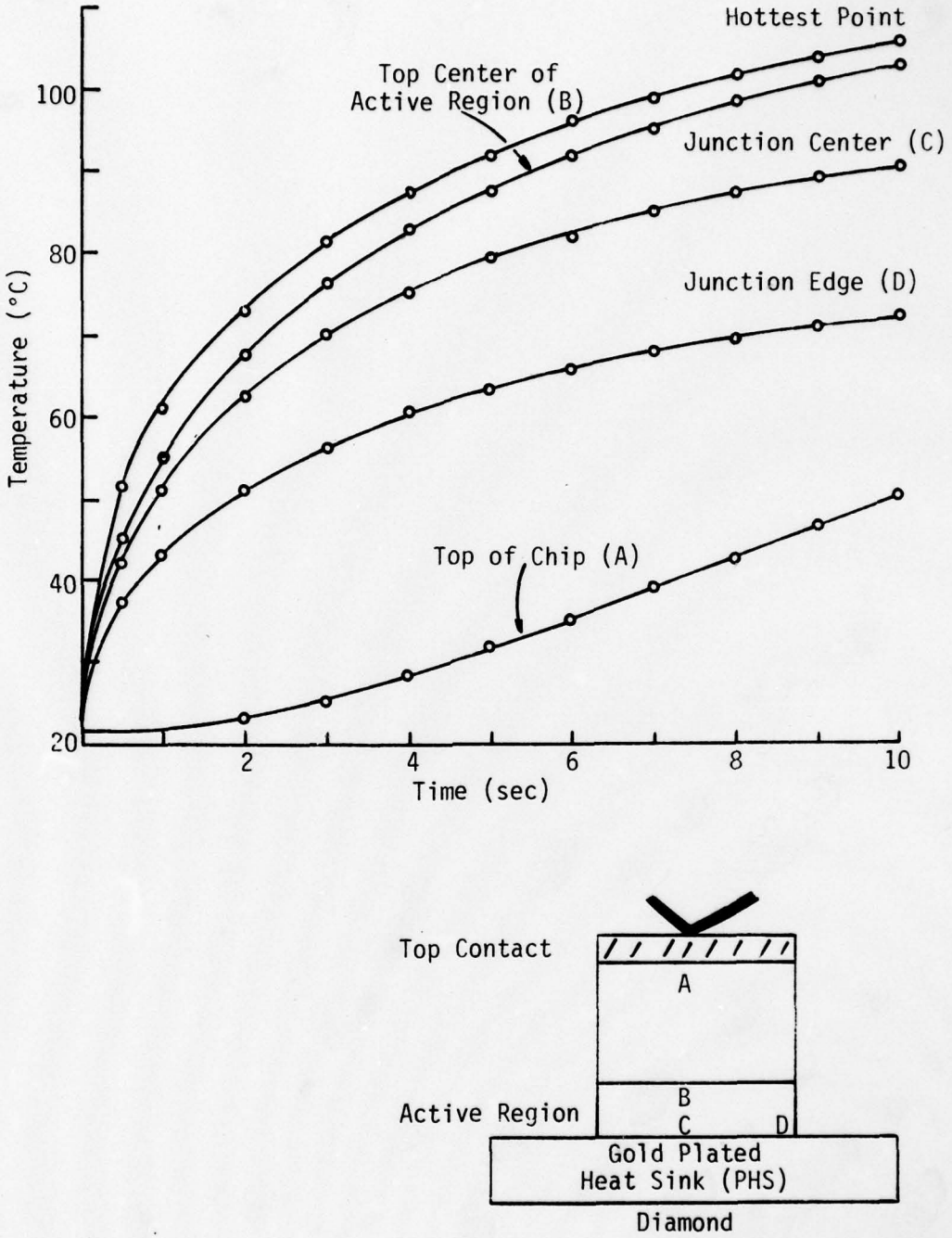


Figure 4. Temperature Response at Different Locations Within Device.

the hottest point moves out to point B. Figure 5 compares the temperature rise for a PHS device mounted on a diamong chip with that of an identical device mounted on a similar size copper chip. The curves, for corresponding points, are almost identical during the first 4.0 μsec. Thus, for low duty-cycle operation with pulse widths less than 4.0 μsec, there would be no advantage to the diamond mounting. The diamond mounting, of course, greatly reduces the device temperature for c.w. or high duty-cycle operation. For example, the average steady-state temperature rise within the avalanche region for the device mounted on diamond is 133 °C compared to 232 °C for the device mounted on copper. These rises correspond to thermal resistances of 6.4 °C/W and 11.1 °C/W, respectively.

Of particular interest in the design of multichip devices is the thermal interaction among chips. From a thermal standpoint, individual chips should be mounted far apart to minimize mutual heating effects among chips. From an electrical standpoint, however, the chips should be mounted close together to minimize inductive effects of connecting leads. A knowledge of the thermal characteristics of multichip devices mounted on diamond chips is desirable, therefore, in order to properly evaluate the electrical and thermal tradeoffs involved in the design of multichip devices.

Figure 6 shows a typical curve for estimating the thermal interaction between two chips for different chip spacing. The curves show temperature profiles across the top surface of the diamond due to heating from the uniformly doped device. For a chip spacing between centers of $a = 4\ r_o$, the temperature at the adjacent edge of each chip is increased by approximately

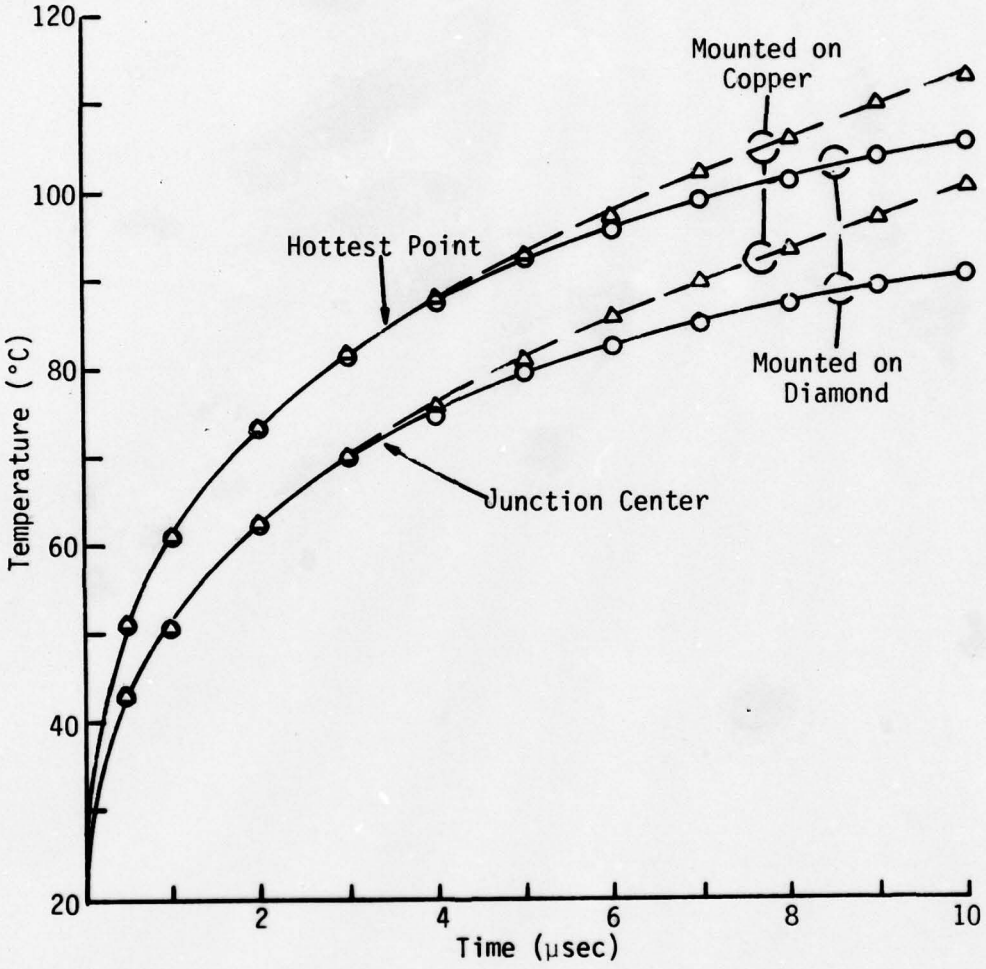


Figure 5. Thermal Response Comparison Between PHS Device on Diamond and PHS Device on Copper.

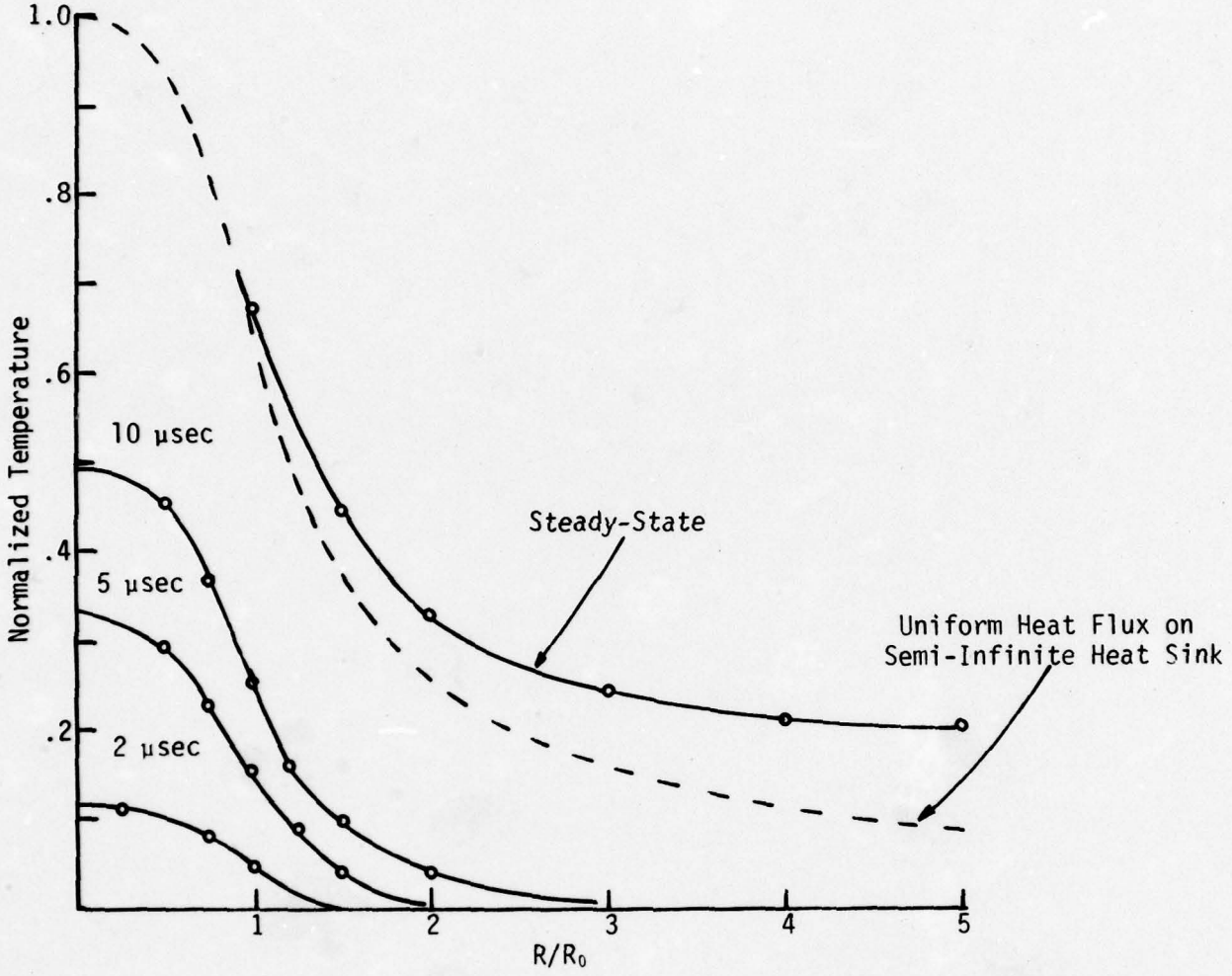


Figure 6. Temperature Along Top Surface of Diamond.

24% while the temperature at the center, which will be the hottest point, is increased by about 21%. These changes reflect a smaller change in the overall thermal resistance of each chip since the temperature drop between the active region of the chip and the top of the diamond can, in some cases, be an appreciable part of the overall thermal resistance.

The time required for heat to diffuse from one chip to another is of utmost importance in determining the transient-thermal interaction of multi-chip pulsed devices. The transient curves of Figure 6 are for the case in which power was applied as a single step function. It is interesting to note that even for spacings of $a = 4\ r_o$ the heat flux due to one chip is just beginning to reach the adjacent edge of the other chip approximately 10 microseconds after the step excitation was applied. For such a spacing, each chip would experience almost no heating effects from adjacent chips during pulses of less than approximately 10 microseconds duration. The quiescent temperature due to mutual heating would, of course, increase slightly, depending upon duty cycle.

Normalized junction temperature and current density profiles in the radial direction within the uniformly doped device are plotted in Figure 7 for selected values of time. The temperature curves are normalized to the maximum steady state value (98.9 °C) at the junction for an input power of 20.9 watts (5 cal/sec) assuming temperature dependent current. Three sets of temperature curves are shown for three different input conditions. The dashed-dotted set corresponds to a constant step in power assuming uniform current density. In an actual device, the total current depends, in part, upon the characteristics of the pulse source; and the current density across the active region is temperature dependent. In practice, the operating

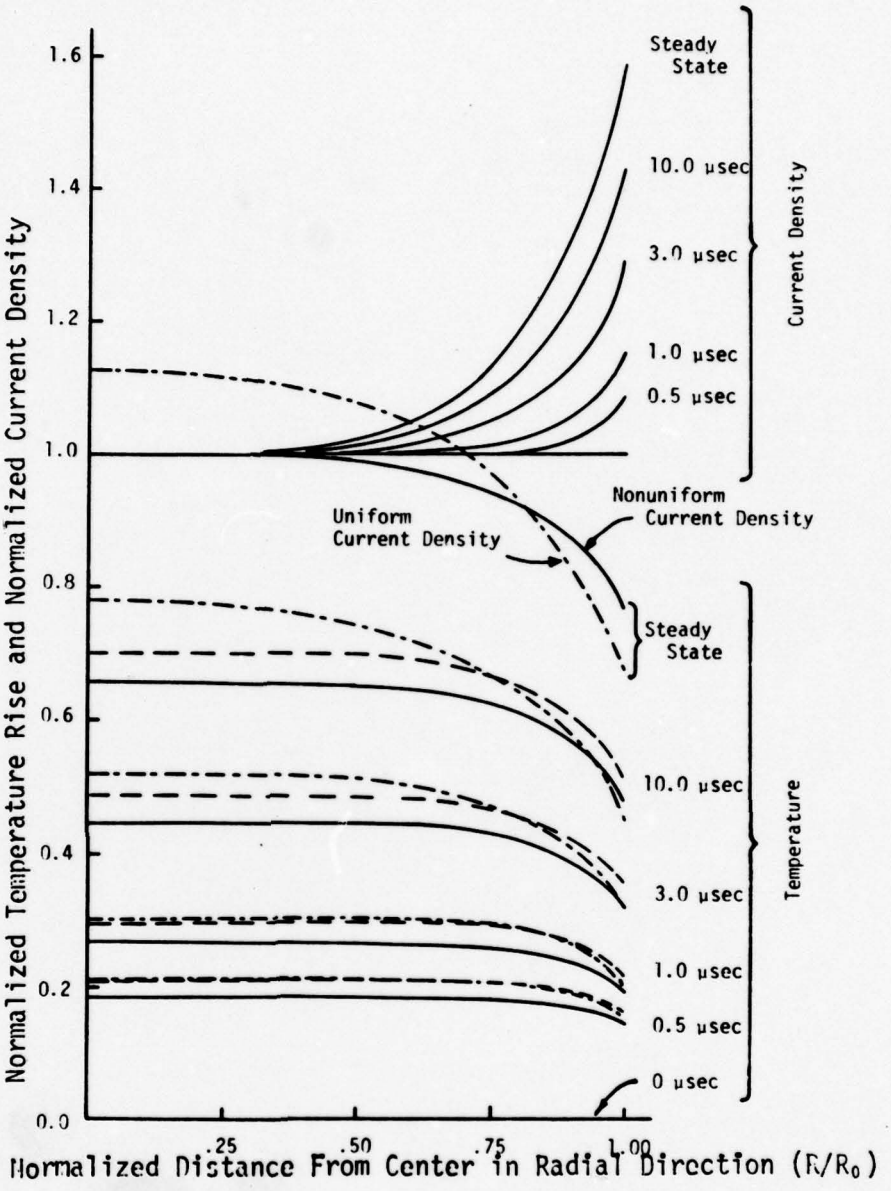


Figure 7. Normalized Temperature and Current Density Across the Junction of Device III on Diamonds at Selected Values of Time. Bias Conditions are: Constant Step in Power, Uniform Current Density — - —, Constant Step in Power, Temperature Dependent Current Density — — —, and Constant Step in Total Current, Temperature Dependent Current Density ————.

characteristics of most IMPATT pulse sources will fall somewhere between these two conditions unless special effort is made to "shape" the current pulse to have an increasing slope. For a constant power step of 20.9 watts, the total current decreased from an initial value of 339 mA at t = 0 to a steady-state value of 294 mA while the voltage increased from 61.6 volts to 71.1 volts. Under a constant current step of 294 mA, the voltage increased from an initial value of 60.9 volts (17.9 watts) to a final value of 71.1 volts (20.9 watts). The dashed-dotted set corresponds to a constant step in power assuming uniform current density.

The temperature curves for the constant power conditions differ little during the first microsecond, but start deviating significantly thereafter. The difference in the temperature curves for the two temperature dependent current cases is primarily due to the lower initial dissipated power for the constant current conditions. The shape of the corresponsing temperature curves are quite similar, resulting in normalized current density curves differing by less than 0.5%. For values of time less than 1 microsecond, the current density is within 10% of its axial value over 85% ($.0 < r/r_o < .925$) of the area. The redistribution of current occurs rapidly thereafter and becomes fairly well established within the first 10 microseconds. The ratio of rim current density to axial current density is 1.09, 1.15, 1.29, 1.42, and 1.58 at 0.5, 1.0, 3.0, 10.0 and ∞ microseconds, respectively.

Relatively little spreading occurs in the PHS since the ratio of its thickness to the device radius and the ratio of its thermal conductivity to that of diamond are both less than 0.25.[13] Consequently, the ratio of rim current density to axial current density is less and the temperature is more uniform if significant spreading occurred within the PHS. On the

other hand, the current density ratio is larger with the PHS than it would be if the device had been mounted directly to the diamond with a minimum layer of gold.

It is interesting to compare the temperature profiles of a PHS device mounted on a diamond with one mounted on copper. This comparison is made in Figure 8 for a step power input of 20.9 watts, where again the curves have been normalized to the steady-state axial temperature rise of the diamond mounted device. For the first 2 or 3 microseconds, there is little difference in the two cases. As the heat flux diffuses into the diamond, the diamond's higher conductivity acts to limit the temperature accordingly. One would therefore expect both devices to perform similarly under short pulse, low-duty cycle operation; however, for long pulse or high duty-cycle operation the diamond device would offer better overall performance.

Normalized axial temperature profiles of the various high-low devices are shown in Figure 9 for constant power, uniform current density conditions. Although the maximum temperature point is located initially at the point of maximum power dissipation, it moves quickly towards the substrate side of the depletion width due to the relatively poor heat conduction path in that direction. As the maximum temperature point moves away from the point of maximum power dissipation, the temperature gradient on the junction side increases monotonically to its steady-state value. The temperature profile at a particular value of time depends predominately on the distribution of dissipated power while the level of the profile depends mainly on the characteristics of the composite heat sink.

For an assumed electric field intensity, the steady-state axial temperature profile can be approximated quite accurately using the one-dimensional

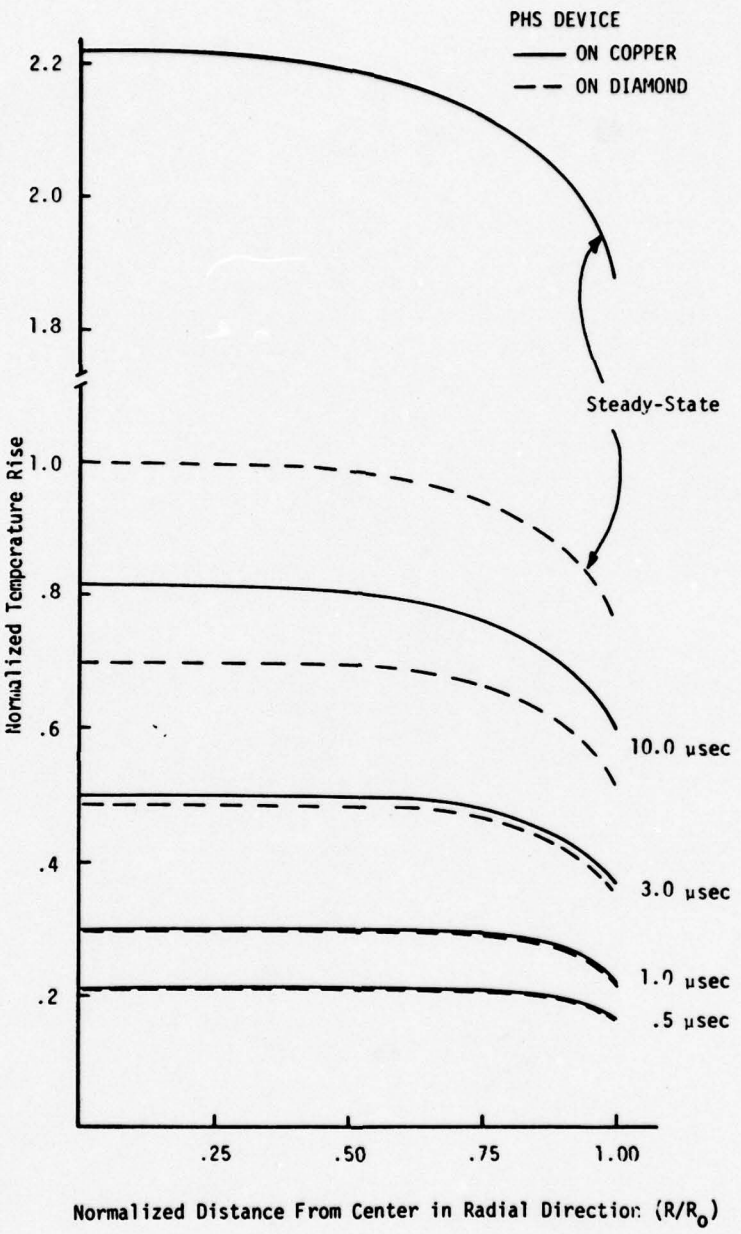


Figure 8. Thermal Comparison Between PHS Device III on Diamond (— — —) and PHS Device III on Copper (———) at Selected Values of Time. Bias Conditions Are: Constant Step in Power, Temperature Dependent Current Density.

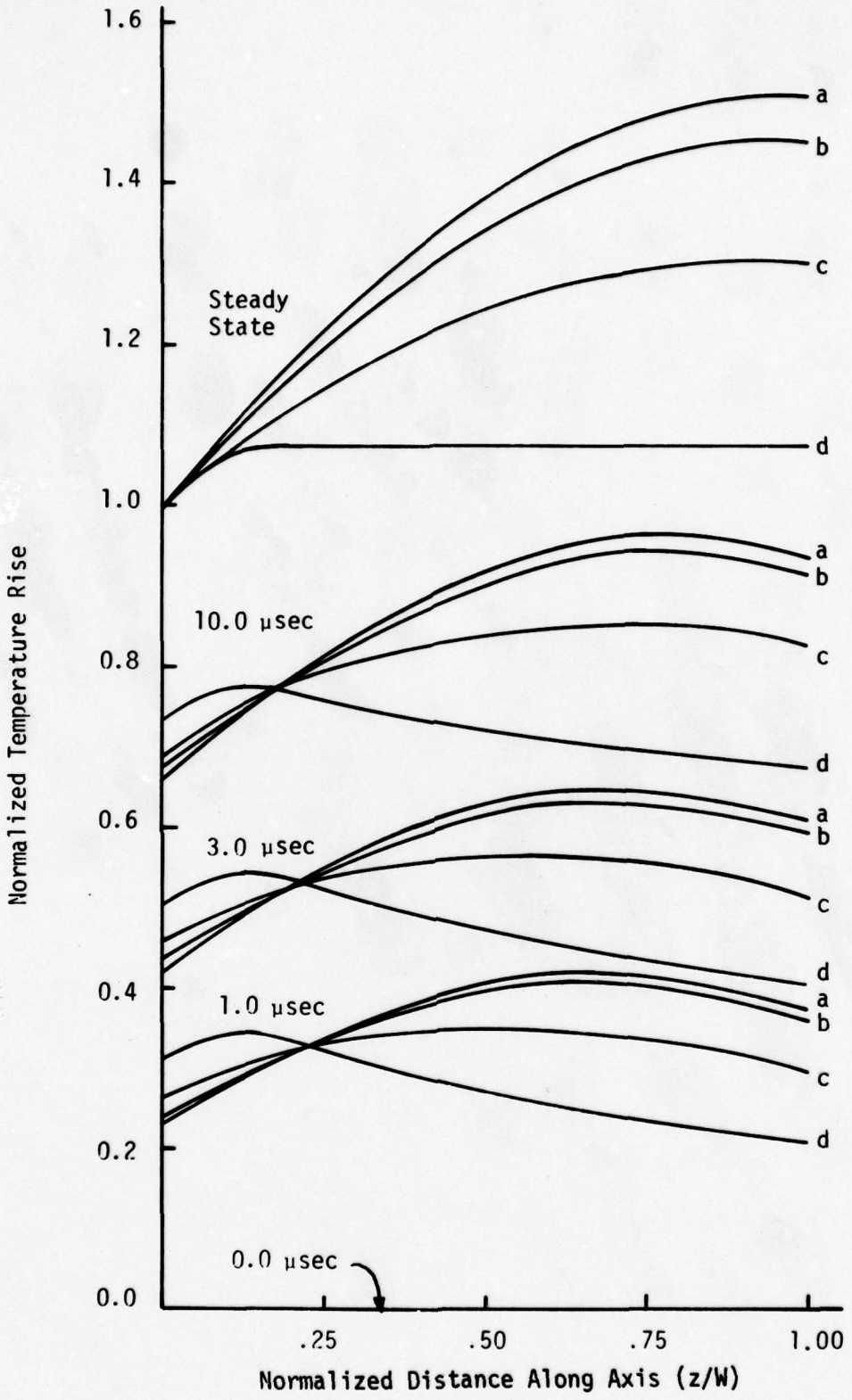


Figure 9. Normalized Temperature Along Axis for Type V PHS Devices a, b, c, and d on Diamond at Selected Values of Time. Bias Conditions are: Constant Step in Power, Uniform Current Density.

heat conduction equation:

$$d^2T/dz^2 = p(z)/kA$$

where p(z) = power density (assuming uniform current density),

K = average thermal conductivity at the expected average temperature, and

A = cross-sectional area.

To illustrate, analytical expressions were derived for three uniformly doped devices designated 1, 2, and 3 of density 1×10^{14}, 8×10^{15}, and 5×10^{16}, respectively. Each device was assumed to have an epitaxial thickness of 3.0 microns. These devices allow a comparison to be made between the analytical approximations and the computer solution, since the electric field intensity of 2 and 3 are identical to III and Vd. The analytical expressions for the three devices, derived assuming negligible heat flow via the top-contact wires, are listed below:

Device 1: Nd = 1×10^{14}, punch through prior to breakdown

$$T(z) = T(o) + \frac{P_{diss}W}{KA}\left(\frac{z}{W}\right)\left[1 - \frac{1}{2}\left(\frac{z}{W}\right)\right], \text{ for } 0 \leq \frac{z}{W} \leq 1.0 \tag{1}$$

Device 2: Nd = 8×10^{15}, punch through at breakdown (PF = 1.)

$$T(z) = T(0) + \frac{P_{diss}W}{KA}\left(\frac{z}{W}\right)\left\{1 - \left(\frac{z}{W}\right)\left[1 - \frac{1}{3}\left(\frac{z}{W}\right)\right]\right\}, \text{ for } 0 \leq \frac{z}{W} \leq 1.0 \tag{2}$$

Device 3: $N_d = 5 \times 10^{16}$, breakdown prior to breakdown (PF = .25)

$$T(z) = T(0) + \frac{P_{diss} W}{KA} \left(\frac{z}{W}\right) \left\{1 - 4\left(\frac{z}{W}\right)\left[1 - \frac{4}{3}\left(\frac{z}{W}\right)\right]\right\}, \text{ for}$$

$$0 \leq \frac{z}{W} \leq .25$$

$$T(z) = T(0) + \frac{P_{diss} W}{KA} \left(\frac{1}{12}\right), \text{ for} \qquad (3)$$

$$.25 \leq \frac{z}{W} \leq 1.0$$

In Figure 10, values calculated from these expressions using a junction-PHS interface temperature T(0) of 129 °C and an average thermal conductivity of .28 watts/cm-°C are compared with the unnormalized steady-state curves of Figure 9. Although the interface temperature was based on the computer results, it could be approximated within 10% using the methods of Holway and Alderstein.[14] As seen, there is excellent agreement between the analytical approximations for devices 2 and 3 and the computer calculations for devices III and Vd.

The computer-derived temperature profiles were used with the temperature dependent ionization coefficients in the electric field calculations. For a given doping profile, the breakdown voltage depends primarily on the average temperature within the avalanche region which, for the profiles considered, corresponds closely to the temperature at the center of the avalanche region. The arrows in Figure 10 indicate isothermal temperatures at which the breakdown voltage is the same as that of the actual temperature profiles. At these higher temperatures, the avalanche widths of devices III and Vb had increased to .92 microns and .99 microns, respectively, from the ambient temperature values of .89 microns and .37 microns.

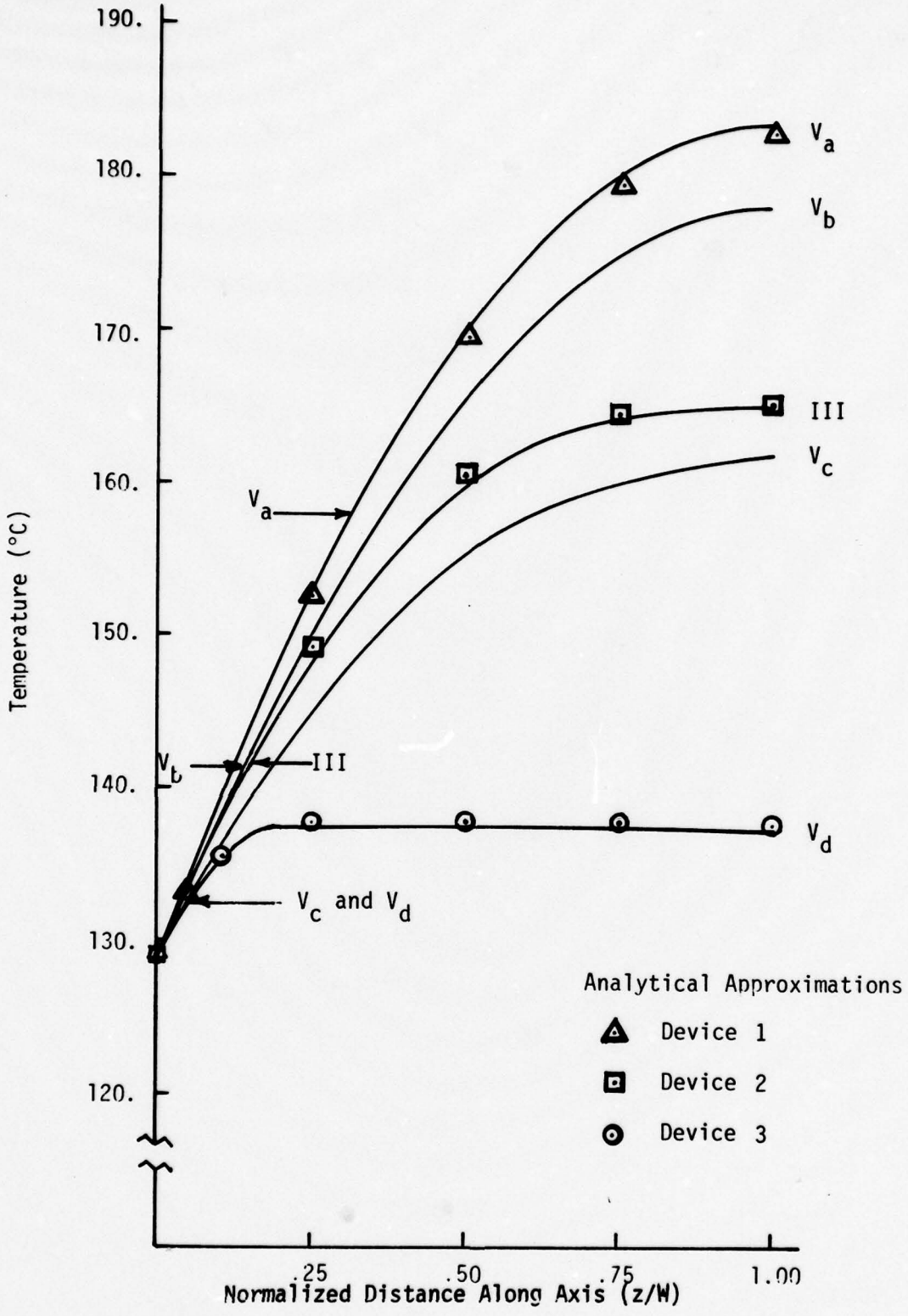


Figure 10. Actual Steady-State Temperature from Computer Results and from Analytical Approximations. Bias Conditions are: Constant Power, Uniform Current Density.

The temperature at the edge of the active region for device Vb is considerably higher, about 25%, than it is at the center of the avalanche region.

CONCLUSIONS

The data presented in this section illustrate the internal transient temperature and current distributions which take place within the active region of PHS IMPATTs of the types considered. In general, the c.w. or high-duty cycle pulsed thermal characteristics of these devices are greatly improved when mounted on diamond. For low-duty cycle pulsed operation where the average device temperature is low, the improvement realized in mounting a PHS device on a diamond vs another material depends upon the pulse length (τ) and the thickness of the PHS. As a "rule-of-thumb", these investigations suggest that when $\tau \leq H^2/\alpha$ (where H is the thickness and α is the diffusivity of the PHS material) no significant advantage is realized in the diamond mounting for low duty-cycle operation.

The temperature at the substrate edge of the highly-efficient high-low structure was found to be significantly higher than at the center of the avalanche region. The same would be true of any highly efficient IMPATT structure in which the ionization is highly localized and the electric field within the drift region is sufficiently high to prevent unsaturated drift velocity and depletion layer modulation under high power operation. One should be aware of these temperature gradients when using a measured "device temperature" to interpret temperature related phenomena effecting reliability such as solder "creep" thermal stresses, etc. A breakdown voltage vs temperature calibration curve, predetermined under isothermal conditions, is usually used in making such measurements. The device temperature thus obtained will invariably be the average temperature

of the avalanche region. The temperature profile within the active region and, hence, the temperature of other points relative to the "measured temperature" can be approximated for devices of known doping by the methods outlined here.

SECTION III

ELECTRONIC MODEL

INTRODUCTION

In this section, the system of differential equations describing the macroscopic behavior of holes, electrons, and electric field within an IMPATT device are given. These equations contain temperature-dependent material parameters which in general are also field dependent. Unfortunately, the most important material parameters, the ionization rates and drift velocities, are not well known at high-field levels where lo-hi-lo and hi-lo devices operate. Device simulations based on these equations often use parameter values extrapolated from low-field measurements.

Quantitative agreement between measured and calculated r.f. characteristics of these devices, however, requires an accurate knowledge of both the structural and the material parameters. The two are so critically related that good agreement is achieved only when "effective" material parameters for a given structure are determined experimentally. The accuracy of the parameters thereby obtained will depend, of course, upon the accuracy of the structural model and the analytical methods used to relate the measurable parameters thereof to the material parameters.

The analytical methods chosen to represent the thermal-electronic interactions are discussed in this section. They are based on a modified Read model that establishes relationships between equivalent circuits and analytical expressions. Experimental d.c. and small-signal admittance data are used to evaluate the temperature-dependent electronic parameters of the circuit model. From these, effective values of important temperature dependent material parameters are deduced. Values of material param-

eters, thus obtained, are compared in Section IV with data previously published in the literature.

FUNDAMENTAL EQUATIONS

The fundamental equations are Poisson's equation, the continuity equations for holes and electrons, and the transport equations for holes and electrons. In one dimension, these can be written as:

$$\frac{\partial E}{\partial x} = q/\varepsilon(p - n + N_d - N_a),$$

$$\frac{\partial p}{\partial t} = -1/q\frac{\partial J_p}{\partial x} + \alpha_p p v_p + \alpha_n n v_n$$

$$\frac{\partial n}{\partial t} = 1/q\frac{J_n}{\partial x} + \alpha_p p v_p + \alpha_n n v_n \qquad (4)$$

$$J_p = q v_p p - q D_p \frac{\partial p}{\partial x}, \text{ and}$$

$$J_n = q v_n n + q D_n \frac{\partial n}{\partial x}$$

where

p = hole density (cm^{-3})

n = electron density (cm^{-3})

J_p = hole current density ($A - cm^{-2}$)

J_n = electron current density ($A - cm^{-2}$)

α_p = ionization rate for holes (cm^{-1})

α_n = ionization rate for electrons (cm^{-1})

v_p = hole velocity ($cm - sec^{-1}$)

v_n = electron velocity ($cm - sec^{-1}$)

D_p = hole diffusion coefficient ($cm^2 - sec^{-1}$)

D_n = electron diffusion coefficient ($cm^{-2} - sec^{-1}$)

q = electronic charge (Coulomb)

ε = dielectric constant (F - cm^{-1})

t = time (sec)

Numerous methods of obtaining the small-signal and/or the large-signal electrical characteristics of IMPATTs from these fundamental equations have been described in the literature. The computational techniques can generally be classified into two broad categories. One category divides the device into two distinct regions—an avalanche region and a drift region. For each region, approximate solutions are found and then combined to form a final solution. Various additional simplifying assumptions are usually made in order to obtain analytical solutions within each region. The principle assumptions are: ionization rates and drift velocities for holes and electrons are equal, the variations about the quiescent values are small, and the diffusion terms are neglected.

The other category includes those methods in which the equations are solved numerically without introducing any simplifying assumptions. The most general methods of this type involve finite difference equations in which the solution starts with initial conditions and proceeds through the transient to a final steady-state solution. Fourier analysis of the steady-state waveforms then leads to output power, efficiency, and admittance data.

Initially, a comprehensive numerical solution of the latter category was attempted in which all temperature-dependent parameters known to effect device performance were included. Although considerable effort went into this solution, it was finally abandoned in favor of a more tractable solution for the following reasons:

1) Incorporating thermal effects as functions of time into such solutions, although straightforward, proved to be extremely expensive.

2) The electrical characteristics of lo-hi-lo devices are ultra critical to structural and material parameters. At present, there is some dispute about the values of drift velocities and ionization rates of GaAs at high field levels. It was found that these parameters are not adequately known to justify the added expense and complexity of such a solution.

3) Cause-and-effect relationships and equivalent circuit models, important design aids for the development engineer, are difficult to determine with general computer solution because of the many parameters involved.

As the program progressed, a modified Read diode approach was chosen based on the small-signal analytical theory of Gilden and Hines,[15] Gummel and Blue,[16] Misawa,[17] and Fisher[18] and on the large-signal analytical formulation of Decker.[19] This approach resulted in a conceptually simple, empirically based model which included important temperature-dependent parameters. The material and structural parameters of the model and their dependence on temperature were determined experimentally from measured d.c. and small-signal admittance data as described in Section IV. The material parameters obtained by curve fitting experimental data to the models described in this section are also compared to previously reported data in the next section.

CIRCUIT MODEL

A qualitative agreement between measured and calculated microwave characteristics is vital to a realistic treatment of the effects of temperature on the operating characteristics of IMPATT oscillators. Initial admittance simulations of a lo-hi-lo device using the general small-signal theory of Gummel and Blue[16] and the often accepted ionization coefficients of Hall and Leck[12] gave poor quantitative agreement with experimental data. Because of the many parameters involved in a general computer analysis, it

was not possible to achieve self-consistent agreement between the simulated and experimental data for both d.c. and r.f. conditions.

Since such an analysis gives little insight into what actually occurs within the device, a more retractable analysis was chosen based on a simplified model. This latter approach proved to be more useful in relating the various intereactions among structural parameters, material parameters, and operating characteristics. Temperature-dependent parameters of the lo-hi-lo structures were experimentally determined using an equivalent circuit of a modified "Read" diode.

The idealized "Read" model, depicted in Figure 11, separates the diode into two distinct regions: a vanishingly narrow avalanche region in which carriers (holes and electrons) are generated through impact ionization and a much wider drift region in which one carrier type drifts at saturated velocity. Although the equivalent circuit of this model contains no resistive elements (in contrasts to the modified circuit described later), the overall circuit impedance exhibits a negative real part above a certain frequency called the "avalanche" frequency. The negative resistance can be attributed to two distinct phenomena. In the avalanche region, the generation rate of carriers is proportional to the density of carriers and to the electric field.

Assume that a small sinusodial voltage at a sufficiently high frequency is superimposed across a device biased to breakdown. Also assume that the field within the avalanche region is in phase with this voltage. The density of carriers or current, J_c, will increase exponentially with time whenever the r.f. and d.c. fields exceed the breakdown or critical field, E_c. They will decrease exponentially with time whenever the fields fall below E_c. This is depicted in Figure 11 and

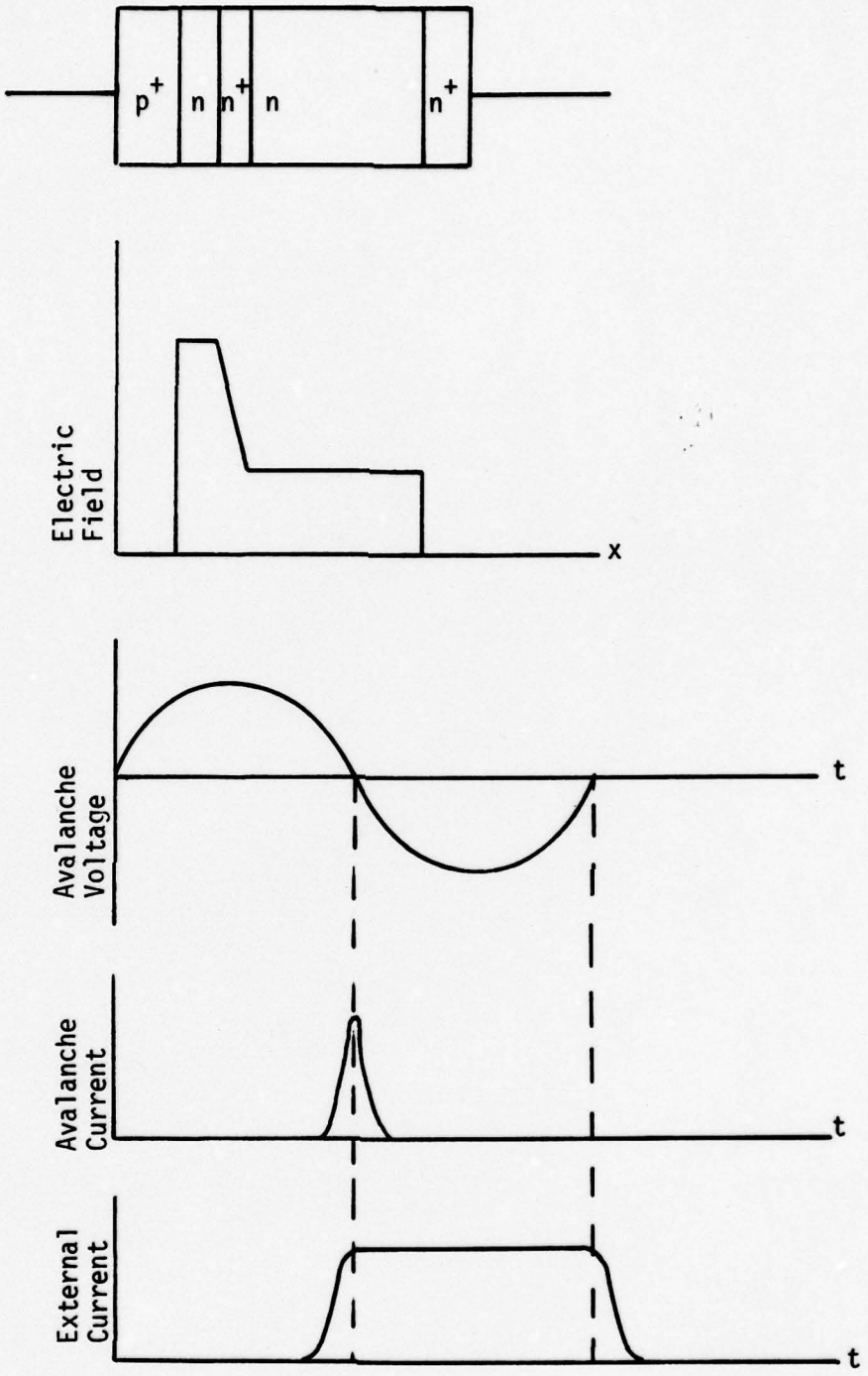


Figure 11. Lo-hi-lo Diode Structure, Field Profile, a.c. Voltage and Current Waveforms

results in the current density generated within the avalanche region lagging the r.f. field, or terminal voltage, by 90°. The total current consists of this inductive component and a displacement component. Thus, the avalanche region can be represented by a parallel LC circuit with the avalanche frequency being defined as $\omega_a = (LC)^{-2}$.

The equivalent circuit shown in Figure 12 can readily be obtained from the fundamental equations if the following assumptions are made:

- diffusion terms are negligible,
- ionization rates and drift velocities for holes and electrons are equal,
- the total current in the avalanche region is independent of position.

An impedance expression can readily be derived from this circuit if one notes that

$$I_T = j\omega C_d V_d + \beta I_a$$

where

$$I_a = I_T \frac{1/j\ L_a}{j\omega C_a + 1/j\omega L_a} = I_T \frac{Z_a}{j\omega L_a}$$

Sutstituting I_a into the above equation and using the relationship that $V_d = V_T - V_a = V_T - Z_a I_T$ one obtains

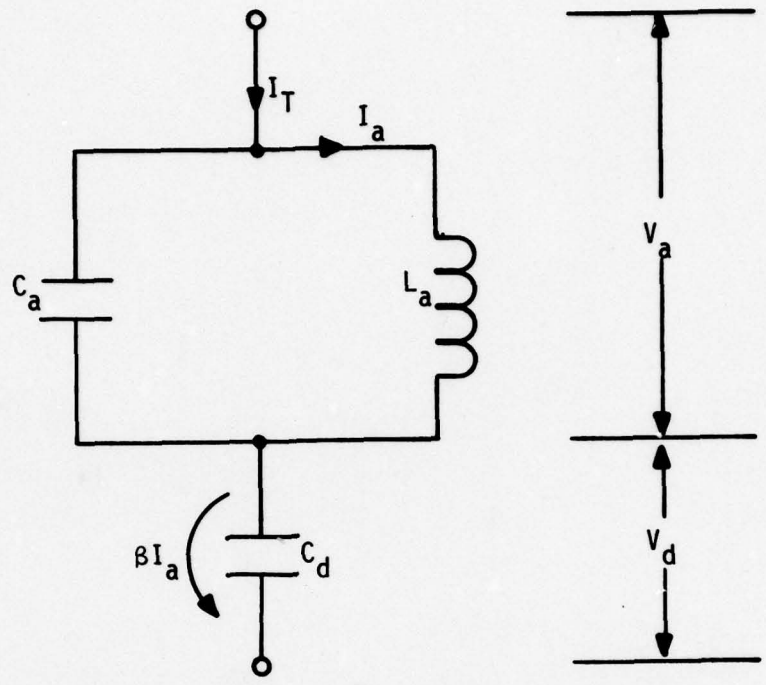
$$I_T = j\omega C_d (V_T - Z_a I_T) + \frac{\beta Z_a}{j\omega L_a} I_T$$

or

$$Z_D(j\omega) = (1 - \beta' F)/j\omega C_T \qquad (5)$$

where

$$\beta' = l_a/l_T + \beta l_d/l_T \quad \text{and}$$



$$C_a = \varepsilon A / l_a \qquad L_a = l_a / 3\bar{\alpha}' v I_0$$

$$C_d = \varepsilon A / l_d \qquad \beta = \frac{1 - \exp(-j\Theta_d)}{j\Theta_d}$$

Figure 12. Equivalent Circuit of Read Diode.

$$F = 1/(1 - \omega^2/\omega_a^2).$$

Expression [5] is equivalent to the small-signal impedance expression given by Gilden and Hines[15] which has been used by others[21,22] to investigate the effect of temperature on the admittance of uniformly doped and hi-lo doped Schottky GaAs structures. The expression does not, however, adequately represent the measured admittance data of the lo-hi-lo GaAs devices studied during this program, especially about the avalanche frequency. This is illustrated in Figures 13 and 14 for two typical x-band structures. The doping profile of the material from which diode type A was constructed showed a highly doped "spike" located approximately 2500 Å from the junction with a maximum doping concentration of 3.5×10^{17} cm^{-3} while that of diode B showed 1700 Å and 6.5×10^{17} cm^{-3}. The avalanche region of diode B is considerably narrower than that of A; yet its admittance differs more from the idealized model than that of A. For a more accurate description of the measured behavior, one must resort to the more generalized, but less retractable, model or one must modify the idealized model to include "second order" effects.

Initial investigations along the latter lines suggested that the differences could be accounted for by adding a small real part to the avalanche zone admittance, i.e., by modifying the Read diode circuit model to include a resistance in series with the avalanche inductor. Hunlin, et al.[23] have introduced an equivalent circuit in which two resistive elements were added. These represent the effects of unequal ionization rates, unequal drift velocities, finite avalanche widths, excess saturation current and/or tunnel current, etc. The functional dependence of these elements on structural and material parameters were obtained from approximations of a more general analysis.

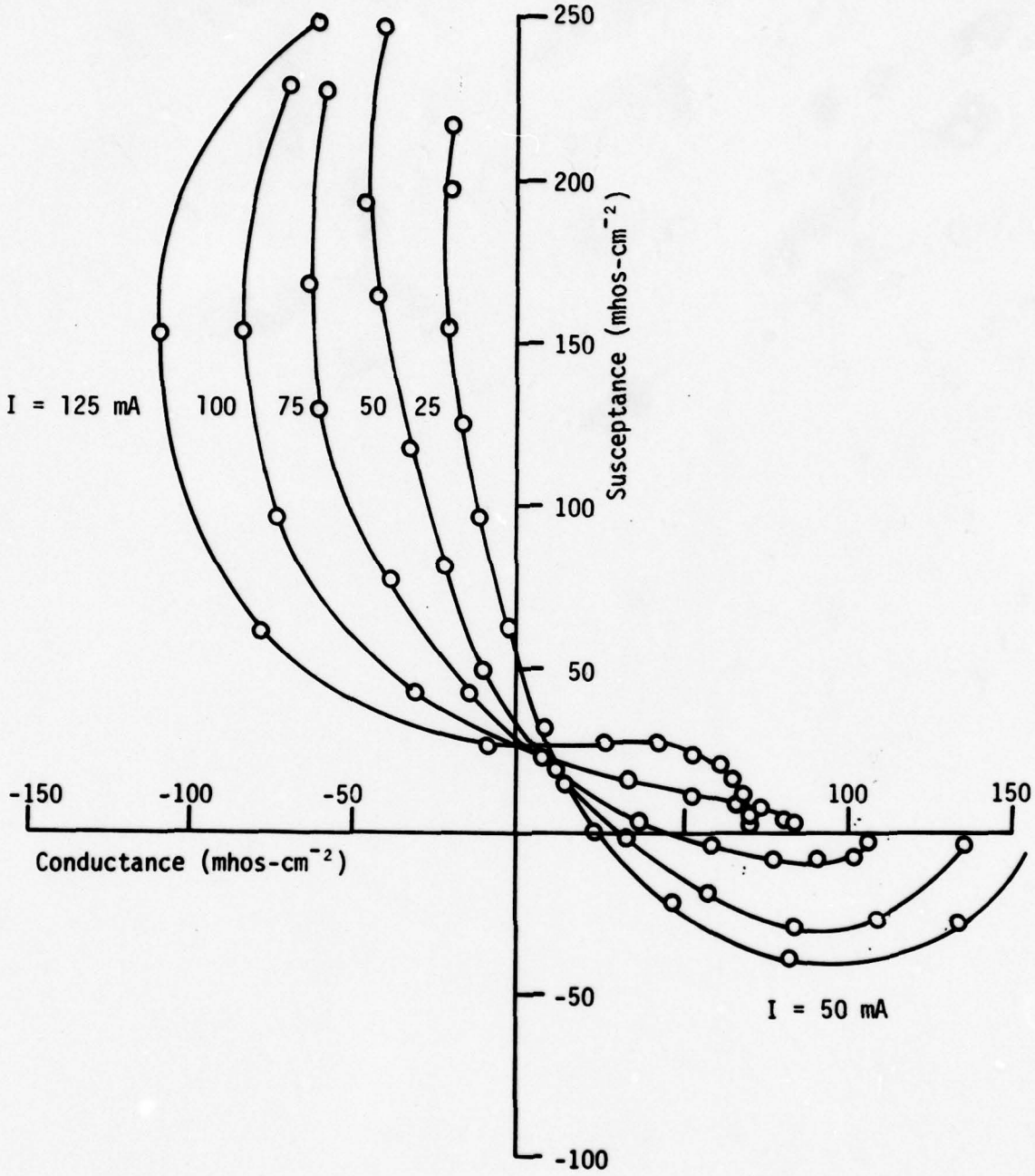


Figure 13. Measured Small-Signal Impedance of lo-hi-lo Structure with $l_p \sim 2500$ Å.

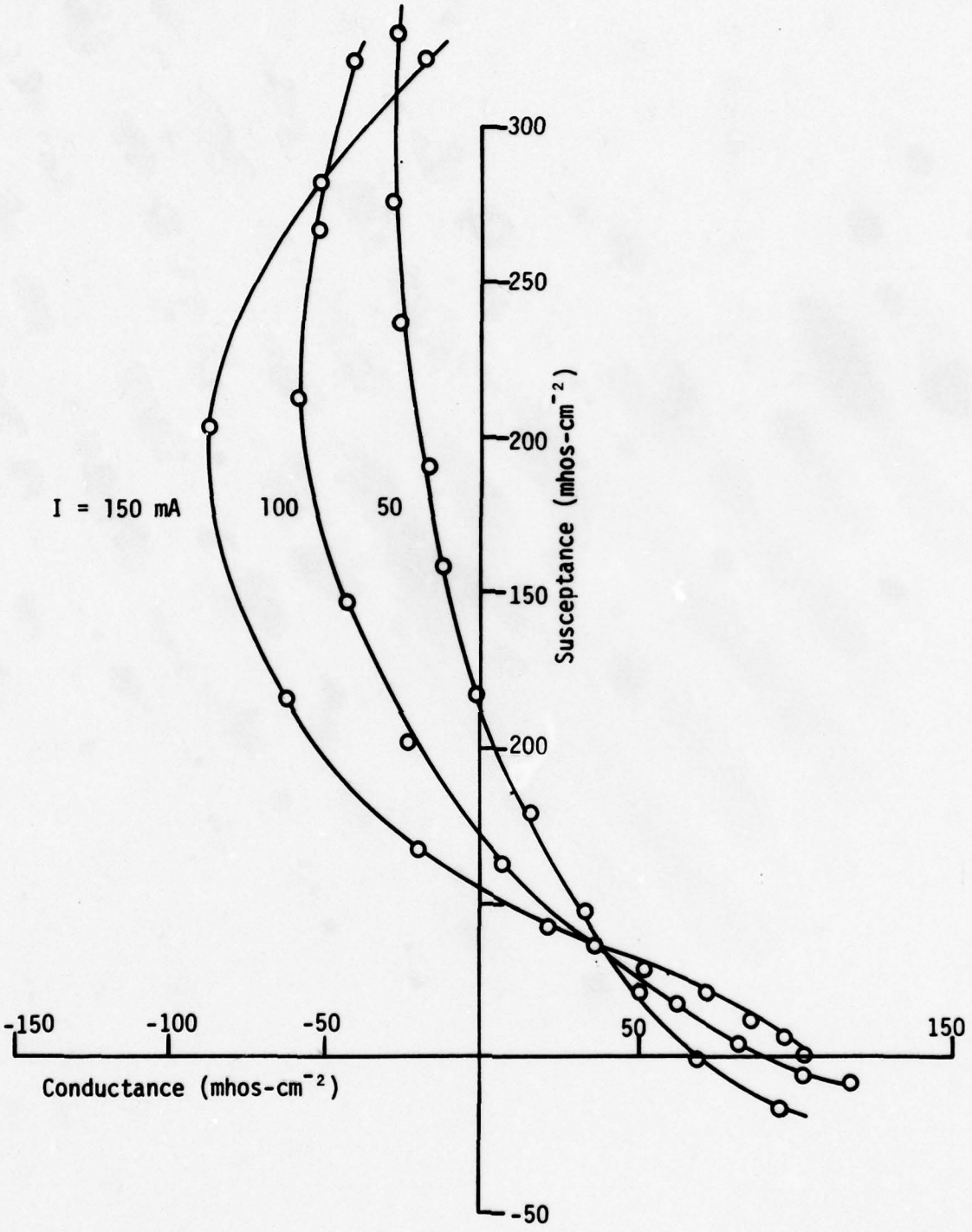


Figure 14. Measured Small-Signal Impedance of lo-hi-lo Structure with l_p ~ 1700 Å.

Misawa[24] shows, qualitatively, how various field profiles and carrier generation distributions within the space-charge region effect its differential conductance (dI/dV). In general, an increase in current requires an increase in the generation of carriers. As a result of this increase, the electric field profile changes. If the change in electric field profile for an increase in current is such that the voltage increases, (i.e., the integral of the electric field over the space-charge region decreases), then the differential conductance is negative. Conversly, if the change in electric field profile for an increase in current results in an increase in voltage, then the conductance is positive.

These effects introduce an additional element within the avalanche equivalent circuit which can be modeled as a parallel conductance. The functional form used in describing this element is based on Gummel and Blue's[16] and Misawa's[17] low-frequency approximation for a silicon device in which the electric field was assumed uniform across the avalanche region. A low-frequency expansion of the avalanche admittance in both analyses show a negative real part equal to $-\bar{\alpha}' I_0/5$. Misawa[17] further demonstrated, via computer simulations, that the negative conductance was relatively independent of frequency over a decade of frequency centered about the avalanche frequency. A parallel conductor of value $-k_1\bar{\alpha}' I_0/5$ was added, where k_1 is a factor dependent upon the relative magnitudes of the ionization coefficients and their derivatives.

Phenomenologically, the effect of excess saturation and/or tunnel currents add positive damping to the avalance processes. The functional form for this effect was taken from the analysis of Fisher[18] who obtained closed-form analytical expressions for the r.f. carrier current density for limiting cases. One such case applies when $\alpha_n \sim \alpha_h$. The carrier current then becomes

$$\tilde{J}_c = \tilde{E}_a J_0 \frac{(\alpha_e' + \alpha_h')/(\alpha_e + \alpha_h)}{1/M + j\omega l_a/3v} .$$

Denoting

$$(\alpha_e' + \alpha_h')/(\alpha_e + \alpha_h) = \bar{\alpha}'/\bar{\alpha},$$

one obtains

$$\tilde{J}_c = \frac{\tilde{E}_a}{\bar{\alpha}/\bar{\alpha}' J_0 M + j\omega l_a \bar{\alpha}/3\bar{\alpha}' v J_0}$$

or

$$\tilde{I}_c = \frac{V_a}{1/\bar{\alpha}' I_0 M + j\omega l_a/3\bar{\alpha}' v I_0} = \frac{V_a}{R_s + j\omega L_a}$$

where

$$L_a = l_a/3\bar{\alpha}' v I_0 ,$$

$$R_s = 1/\bar{\alpha}' M I_0 ,$$

$$\tilde{V}_a = \tilde{E}_a l_a , \text{ and}$$

$$\tilde{\alpha} l_a = 1 \text{ (dc condition for breakdown for } M \gg 1).$$

Thus, another resistive element must be included in series with the avalanche inductance to account for finite multiplication. The complete modified Read circuit model is shown in Figure 15.

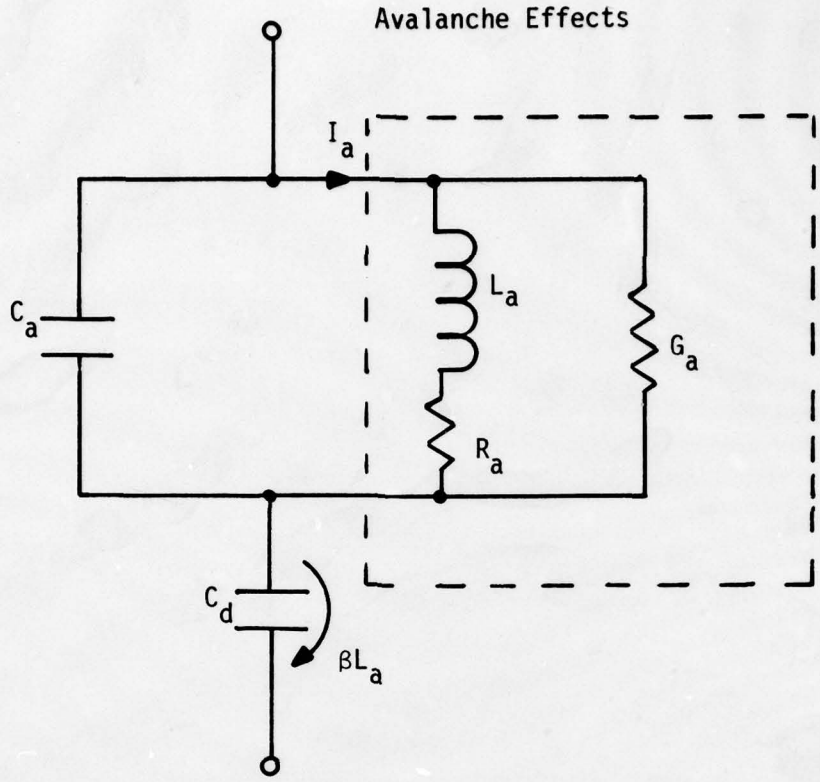
The total small-signal impedance of the modified circuit, expressed as a function of the complex frequency s, is

$$Z_D(s) = Z_a(s) + \frac{1}{sC_a}[1 - F(s)\beta'(s)]$$

where

$$z_a(s) = \frac{1}{sC_a + G_a + 1/(R_a + sL_a)} ,$$

$$F(s) = \frac{G_a + 1/(R_a + sL_a)}{sC_a + G_a + 1/(R_a + sL_a)} ,$$



$$C_a = \varepsilon A/l_a \qquad L_a = l_a/3\,\bar{\alpha}'vI_0$$

$$G_a = k_1\bar{\alpha}'I_0/5 \qquad R_a = k_2/\bar{\alpha}'MI_0$$

$$C_d = \varepsilon A/l_d \qquad \beta = \frac{1 - \exp(-j\Theta_d)}{j\Theta_d}$$

Figure 15. Modified Read Diode Model.

and

$$\beta'(s) = \frac{1 - \exp(-s\tau_d)}{s\tau_d} .$$

The above expression also assumes a relatively narrow avalanche region and neglects the phase angle between the carrier current entering the drift region and that flowing through the plane where the lumped elements are defined. The small-signal impedance can be rewritten as

$$Z(s) = \frac{1}{sC_T}[1 - F(s)\beta'(s)]. \qquad (6)$$

Gummel and Scharfetter[20] showed that an expression of this form fitted numerical results obtained by a more general analysis for a current ratio factor F(s) of the form

$$F(j\omega) = \frac{(i\omega - B)}{(i\omega - A)(i\omega - A^*)} \frac{AA^*}{-B} \qquad (7)$$

where * denotes the complex conjugate and A is the complex natural resonant frequency

$$A = \omega_r + i\omega_a$$

B is real and denoted by

$$B = -\omega_c .$$

Equivalent forms of expression [6], or appropriate approximations thereof, were used extensively throughout the program to correlate theoretical and experimental data. One approximation which was found to be most useful assumes the added terms are small, i.e., $\omega L_a >> R_a$ and $\omega C_a >> G_a$. Under these conditions, the factor (F(jω) becomes

$$F(j\omega) \sim \frac{1}{1 - \omega^2/\omega_a^2 + j\omega(R_a C_a + G_a L_a)}$$

and the admittance becomes

$$Y(j\omega) = j\omega C_T \frac{1 - \omega^2/\omega_a^2 + j\omega(R_a C_a + G_a L_a)}{\bar{l}_d - \omega^2/\omega_a^2 + j\beta\bar{l}_d + j\omega(R_a C_a + G_a L_a)} \qquad (8)$$

Admittance data calculated with this expression are in excellent agreement with that obtained by more exact methods. Furthermore, it is relatively easy to use this expression to approximate the values of the circuit elements by curve fitting measured or theoretical data. For example, Figure 16 compares data calculated with expression with the data of Gummel and Scharfetter[20] for a silicon device. As seen, there is excellent agreement between the two sets of curves over a large frequency range. These curves are typical of silicon abrupt junction devices and illustrate the differences between their admittances and those of the lo-hi-lo GaAs devices shown in Figure 13. The significant differences occur about the "natural resonant" frequency where the silicon devices exhibit a cutoff* frequency, below the resonant* frequency, contrary to that observed for the GaAs devices. The parameters used in the modified equivalent circuit are tabulated on the next page.

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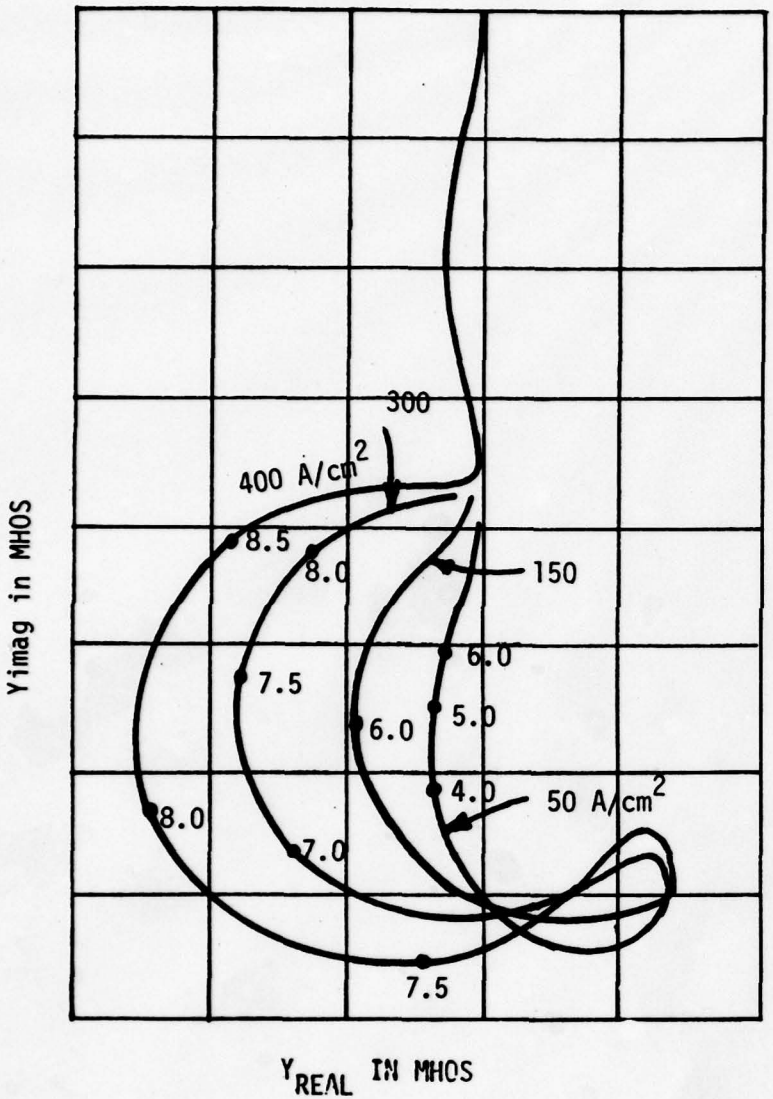
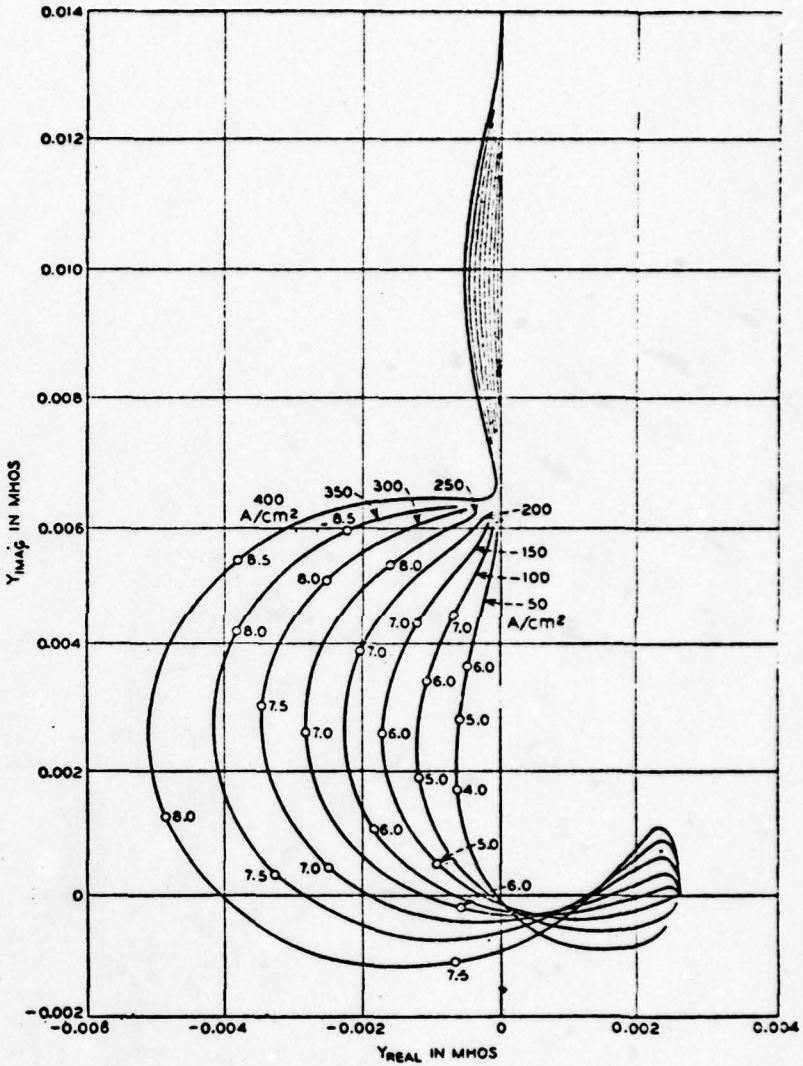
* These terms are taken from Physics of Semiconductor Devices, by S. M. Sze[11] in which the resonant frequency, f_r, is defined to be "that frequency at which the imaginary part (B) of the admittance changes from inductive to capacitive" and the cutoff frequency, f_c, to be "the minimum frequency at which the real part of the admittance changes from positive to negative". Sze further states that "For a Read diode, f_c is exactly equal to f_r. For a general IMPATT diode, it will be shown, however, that f_c is lower than f_r, and that as the avalanche width increases, the difference becomes larger". The admittance behavior observed for the GaAs devices is in contradiction to the last statement.





Admittance of Read diode R1. Selected frequencies, in GHz, are marked off on each curve.

Figure 16. Comparison of Data Calculated with Expression [8] to that Calculated by Gummel and Scharfetter.[20]

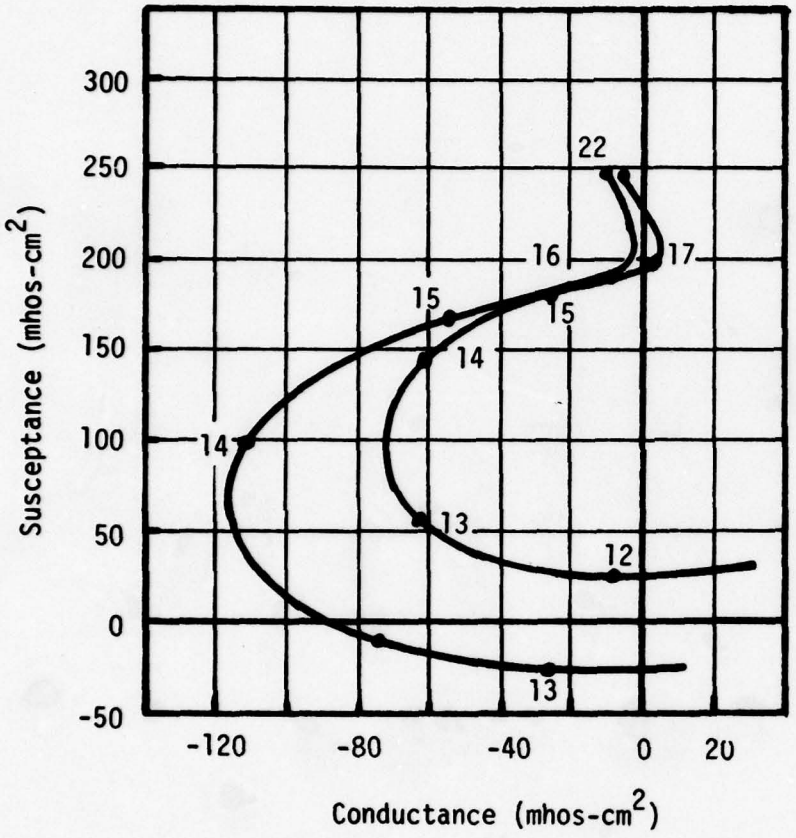
J_0	ϵ_r	ℓ_a	ℓ_d	v	f_a	k_1	k_2	M
A/cm^2		10^{-4}cm	10^{-4}cm	10^7cm/sec	GHz	-	-	-
**	12	1.0	9.0	1.0	**	3/2	1	∞

For each dc current density** a resonant frequency was determined emperically by curve fitting and found to follow:

$$f_a^2(GHz) = .133\ J_0(A/cm^2)$$

Figures 17 and 18 compare data reported by Sudbury and Laton[25] with data calculated with expression [8]. The former data were published to illustrate the differences between the admittances of uniformly doped n-type and p-type GaAs devices when different hole and electron ionization rates are assumed. Using equal ionization rates as reported by Hall and Leck,[12] they found both type devices exhibit an admittance behavior about the natural resonant frequency similar to that for Si, i.e., cutoff frequency below resonant frequency ($f_c < f_r$). Using unequal ionization rates as reported by Stillman, et al.,[26] however, they found the admittance data for the two types to differ significantly.

Specifically, the p-type device was found to exhibit an admittance behavior typical of silicon devices, i.e., $f_c < f_r$. The n-type device, on the other hand, was found to exhibit a behavior similar to the measured admittance of Figure 13, i.e., $f_c > f_r$. By allowing k_1 to be positive or negative, both sets of curves could be closely approximated using expression (5). A negative value of k_1 corresponds to a positive differential resistance arising from space charge effects within the avalanche region. The



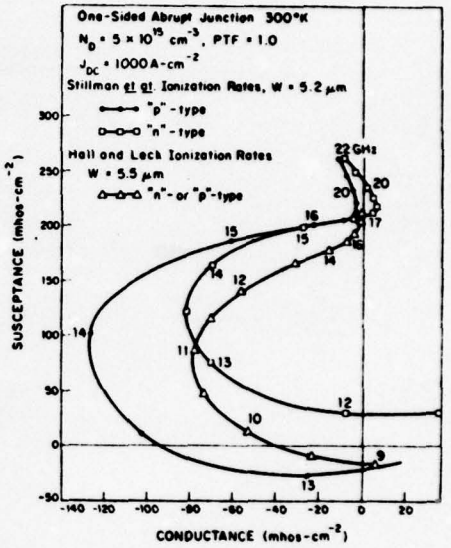


Fig. 2. Small-signal IMPATT admittance for several ionization rates in n- and p-type structures.

Figure 17. Data Calculated from Expression [8] Compared to Data Reported by Sudbury and Laton.[25]

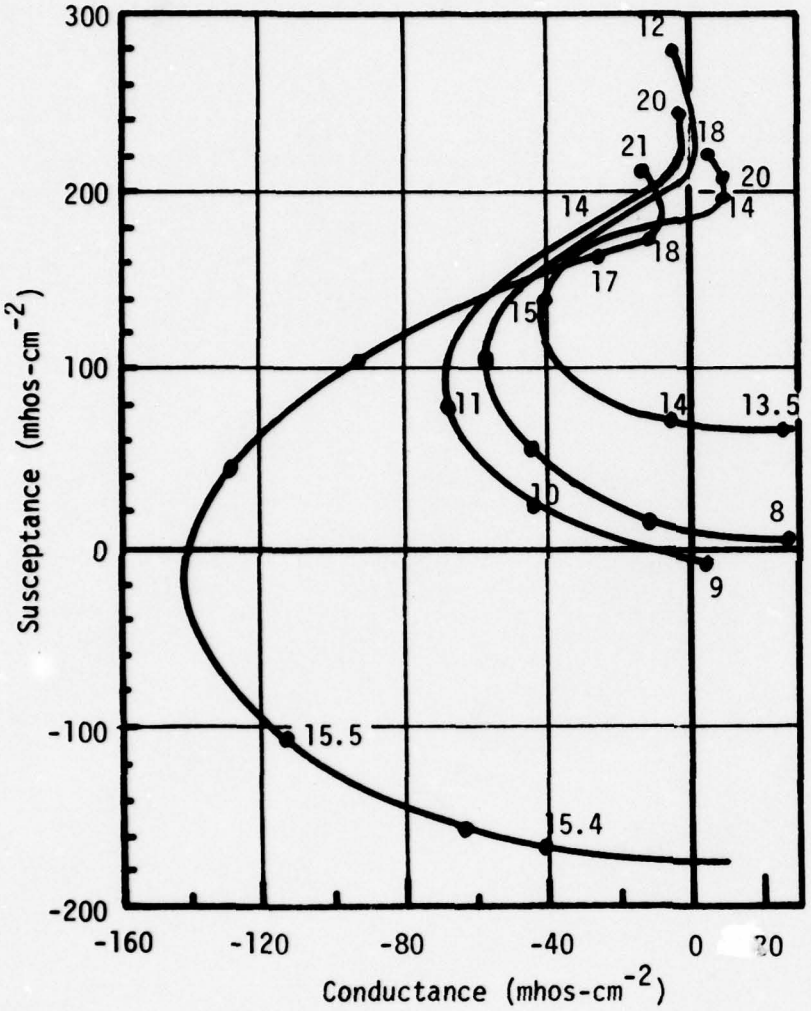


Figure 18. Data Calculated from Expression [8] Compared to Data Reported by Sudbury and Laton.[25]

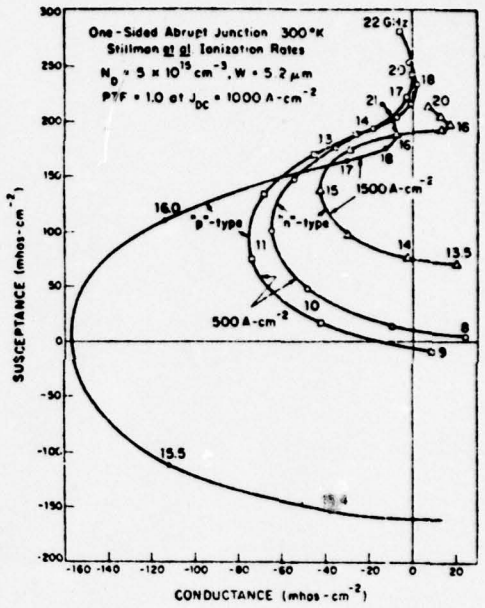


Fig. 3. Small-signal IMPATT admittance for n- and p-type structures for several current densities.

curves on the left side of each figure were calculated from expression [8] and should be compared with the corresponding, more exact curves on the right. The equivalent circuit parameters, found by curve fitting, are listed in the following table:

J	ε_r	ℓ_a	ℓ_d	v	f_a	k_1	k_2	M
A/cm	-	10^{-4}cm	10^{-4}cm	10^{-7}cm/sec	GHz	-	-	-
				p-type				
500	12.5	.9	4.3	.8	9.10	+.6	1	∞
1000	12.5	.9	4.3	.8	12.80	+.6	1	∞
1500	12.5	.9	4.3	.8	15.47	+.6	1	∞
				n-type				
500	12.5	.8	4.4	.8	8.60	-1.5	1	∞
1000	12.5	.8	4.4	.8	11.90	-1.5	1	∞
1500	12.5	.8	4.4	.8	14.00	-1.5	1	∞

Values of f_a were first estimated from the data of Sudbury and Laton and then f_a, ℓ_a and k_1 were simultaneously adjusted to obtain the "best fit" curves. In all cases the total depletion width, $\ell_a + \ell_d$, was kept equal to that determined from static calculations, i.e., 5.2 microns. Since they assumed zero saturation current, M was set infinitely large ($R_a = 0$). Excellent qualitative agreement exists between the corresponding sets of curves.

It should be noted here that the admittance differences are due mainly to the change in sign of the k_1 factor. A negative sign for k_1, such as is indicated for the n-type material, corresponds to a positive conductance G_a. This would imply a complex natural resonant frequency with a <u>negative</u>

real part. On the other hand, k_1 is positive for the p-type corresponding to a negative conductance or a complex resonant frequency with a positive real part.

CONCLUSIONS

Admittance calculations based on generalized small-signal theory could not be brought into agreement with the measured admittance of lo-hi-lo devices. Whether this was due to uncertainties in the material and structural parameters or to effects not included in the theory could not be determined unambiguously because of the many parameters involved in the numerical solution. An approximate analytical model was described in this section which closely approximated admittance calculations obtained by more exact methods. The analytical model contains two elements which cam be adjusted to simulate effects not easily included in the more generalized theory, such as tunneling and/or diffusion.

SECTION IV

EXPERIMENTAL AND THEORETICAL RESULTS

INTRODUCTION

This section describes the methods used to obtain agreement between the calculated and the measured small-signal admittances and the approach used to characterize the temperature-dependent elements contained in the equivalent circuit of Figure 15. For the most part, the discussions are restricted to high-efficiency GaAs lo-hi-lo devices. These proved to be the more difficult to model since the electric field within their avalance region is relatively high in comparison to abrupt junction devices. Their admittance characteristics also showed evidence of high thermionic or tunnel currents. Furthermore, their narrow avalanche regions require breakdown calculations based on the concept of "dark spaces" introduced by Okuto and Crowell.[27-29]

Since the values of many of the physical parameters are uncertain at the high-field levels at which these devices operate, key parameters effecting their breakdown and admittance characteristics were determined by empirical methods. This involved adjusting certain physical parameters to bring theoretically calculated data into agreement with experimental data. This quasi-empirical approach led to a simple, first-order model which could be used in circuit analysis programs to investigate the thermal-electrical interactions of IMPATT oscillators. The circuit model approach also provided an unexpected insight into the operation of IMPATT chips connected in series, as discussed in the latter part of this section.

Upon examining Figure 15, one sees that the major temperature-dependent quantities that effect the circuit elements are the drift width, l_d, the derivitive of the effective ionization coefficient with respect to the

electric field, $\bar{\alpha}'$, the avalanche frequency, ω_a, the effective velocity, $\bar{v}$, the current multiplication factor $\bar{M}$, and the space-charge factor, k_1. These quantities were determined for a number of typical X-band structures either by comparing d.c. measurements with calculations or by curve fitting appropriate admittance expressions to r.f. data.

D.C. CHARACTERISTICS

Experimental data relating to the d.c. thermal-electrical characteristics of a variety of lo-hi-lo devices were compiled. There data consisted of the breakdown voltage at selected temperatures, the temperature coefficient of breakdown, the thermal resistance, and the space-charge resistance. Typical data for a sample of 24 devices constructed from the same wafer using the same processing and mounting techniques are listed in Table III. The material used in these devices is the same as that used in the type B diode described previously. The chips were of gold plated heat sink construction mounted in standard microwave copper stud packages using conventional bonding techniques.

The measured thermal resistances are in good agreement with the theoretical value of 11.1 °C/W obtained with the MITAS II program, considering the latter made no allowance for bonding irregularities and assumed the base of the copper post on which the chip was mounted was maintained at ambient temperature. The spreading resistance from the copper post into a semiinfinite copper heat sink would contribute an additional 2.5 °C/W to the overall thermal resistance of the computer model.

The wide variations in breakdown voltage, temperature coefficient of breakdown, and space-charge resistances are typical of nonpunch-thru lo-hi-lo devices. The depletion width at breakdown depends strongly on the location and maximum concentration of the highly doped spike. Slight

TABLE III

D.C. Characteristics of Type B Devices

Sample Number	V_B Volts	$\Delta V/\Delta T$ Volts/°C	R_T °C/W	R_{SC} Ohms
1	50.5	.11	14.8	53.3
2	50.7	.11	13.5	53.3
3*	27.8	.09	14.5	29.3
4	19.5	.08	16.3	22.7
5	26.3	.09	14.2	37.3
6	26.5	.08	15.0	29.3
7	14.7	.07	16.1	18.7
8	28.3	.10	14.8	42.7
9*	42.3	.10	13.7	53.3
10	26.5	.09	13.9	32.0
11	19.2	.07	13.9	21.3
12*	36.3	.10	13.2	41.3
13	33.6	.10	16.0	48.0
14*	42.1	.11	13.9	44.0
15	42.6	.11	13.1	44.0
16*	35.2	.11	13.3	41.3
17	45.3	.11	13.9	48.0
18	35.0	.10	14.1	36.0
19	34.2	.10	14.3	40.0
20	34.2	.10	16.5	53.3
21*	31.9	.09	13.5	40.0
22	34.7	.11	13.7	53.3
23	35.8	.10	12.7	37.3
24	37.0	.10	14.2	41.3

differences in these values cause large differences in the electric field profiles which lead to large differences in breakdown voltages, depletion widths, and space-charge resistances. These large variations between devices also illustrate the difficulties in accurately modeling their electrical characteristics.

To determine "effective" ionization rates from these data, a computer program was developed for solving the pseudolocal breakdown equations of Okuto and Crowell,[28] i.e.,

$$1 - \frac{1}{M_n} = \int_0^W \alpha_n(E(x,x)\exp\int_x^W [\alpha_p(E(x'),x') - \alpha_n(E(x',x')]dx'dx$$

where

$$\alpha_n(E(x),x) \equiv 0 \text{ for } 0 \leq x \leq D_n$$

$$\alpha_p(E(x),x) \equiv 0 \text{ for } l_a - D_p \leq x \leq l_a$$

Here D_n and D_p are dark space distances which can be intepreted as the distance required to field-accelerate a carrier to its ionization threshold energy, i.e., $D = E_i/qE$. The numerical solution of this equation is straightforward when α_p and α_n are known functions of x(or known explicitly through E(x)).

An accurate knowledge of the doping profile is, of course, crucial if the calculations are to be meaningful. Doping profiles for a subsample of six devices , indicated by asterisks in Table III, were carefully determined using an automatic doping profile. The accuracy of the measurement depends upon properly calibrating the instrument for each diode. Calibration was achieved by two methods and compared. The more conventional method used a

calibration point based on the devices area which was determined from SEM photographs taken from orthogonal directions. The other method was to adjust the calibration point such that the doping density in the drift region corresponded to that specified by the materials manufacturer. The doping profiles obtained by these two methods agreed closely with each other and indicated spike locations which also agreed closely with the nominal location specified by the manufacturer. Since the doping density is not plotted within the zero bias depletion width, it was assumed to be symmetrical about the peak concentration and extrapolated towards the junction.

Initial calculations of breakdown voltage using Stillman's[33] most recent ionization rates (thought at the time to be the most accurate) resulted in calculated breakdown voltages far higher than those measured. Further calculations, using the same rates but adjusting the profiles slightly to simulate possible measurement errors, showed that the discrepancies were unlikely due to errors in the doping profile. Consequently, calculations were made using measured ionization rates of others as tabulated by Stillman.[33] Table IV lists these rates and Table V compares the calculated breakdown voltages obtained with each to the measured values.

As seen, the breakdown voltages calculated with these rates are all significantly different from the measured values. In general, ionization rates are measured on uniformly doped samples and the data fitted to an expression of the form

$$\alpha = \alpha_\infty \exp\{-(b/E)^m\} \text{ with } m = 1 \text{ or } 2.$$

Table IV. Ionization Rate Measurements in GaAs (300°K)(after Stillman).[33]

Reference	$\alpha = a \exp[-(b/E/)^m]$ a	b	m	Method
1. Logan, et al (1962	1.34×10^6	2.03×10^6	2	Diffused p^+-n junctions, assumed $\alpha = \beta$
2. Logan and Sze (1968	3.5×10^5	6.85×10^5	2	Diffused p^+-n and n^+-p junctions $M_{np} \sim M_n \sim$ implied $\alpha = \beta$
3. Kressel and Kupsky (1966)	1.0×10^6	1.72×10^6	1	Vapour phase epitaxial p-n junctions, edge illuminated assumed $\alpha = \beta$
4. Hall and Leck (1968)	2.0×10^5	5.5×10^5	2	Diffused n^+ -p junctions, assumed $\alpha = \beta$
5. Chang and Sze (1969)	4.0×10^6	2.1×10^6	1	Diffused p^+ -n junctions, assumed $\alpha = \beta$
6. Schabde and Yeh (1970)	3.7×10^6	7.2×10^5	2	Liquid phase epitaxial p-n junctions on $Al_{1-x}Ga_xAs$ x = 1, assumed $\alpha = \beta$
7. Salmer, et al (1973)	1.18×10^5	5.55×10^5	2	From avalanche voltage measurements on Schottky-barrier IMPATT devices, assumed $\alpha = \beta$
8. Glover (1973)	$\sim3.5\times10^5$	6.85×10^5	2	Schottky barrier, assumed $\alpha = \beta$
9. McCarthy and Lee (1973)	$\sim3.5\times10^5$	6.85×10^5	2	Schottky barrier, assumed $\alpha = \beta$
10. Stillman, et al (1974b)	1.2×10^7	2.3×10^6	1	Electron ionization coefficient, α } Schottky barrier
	3.6×10^8	2.9×10^6	1	Hole ionization coefficient, β } Schottky barrier
11. Stillman, et al (1975)	2×10^6	2×10^6	1	Electron ionization coefficient α } Breakdown voltage
	1×10^5	5×10^5	1	Hole ionization coefficient β } measurements

Table V. Comparison of Measured Breakdown Voltage with Calculated Breakdown Voltages Using Published Ionization Rates.

		Calculated Voltages Using Published Ionization Rates								
Device No.	Meas. Voltage	1	2,8,9	3	4	5	6	7	10	11
3	27.8	235.4	19.1	36.8	16.4	16.7	6.5	42.6	5.7	86.0
9	42.3	234.3	26.9	46.6	24.5	23.2	6.0	51.6	5.2	89.5
12	36.3	249.7	21.5	42.0	19.8	18.2	5.8	49.4	5.0	93.0
14	42.1	256.0	24.5	45.8	22.6	20.7	5.8	52.9	5.0	95.2
16	35.2	256.0	23.3	43.5	20.7	20.1	6.1	50.4	5.3	93.1
21	31.9	233.8	21.2	40.2	19.0	18.2	6.0	47.5	5.2	87.8

The functional form of this expression can be traced to earlier work of Wolff and Shockly. The work of Wolff assumed high-field conditions where the energy loss to the lattice system is small compared to the energy gained from the field and led to m = 1. On the other hand, Shockly assumed low field conditions where the only particles that contribute to ionization are those which escape phonon scattering and obtained m = 2.

Baraff[30] later pointed out that impact ionization in many materials occur at intermediate fields and formulated an integral equation from which the ionization rate per unit path length could be calculated. His results were presented as normalized universal curves in which $\alpha\lambda$ was plotted as a function of $E_i/qE\lambda$ with various values of E_r/E_i as parameters. Here, E_r is the optical-phonon energy, λ is the mean free path for optical-phonon generation, E_i is the ionization threshold energy, q is the electronic charge, and E is the electric field.

Crowell and Sze[31] obtained an analytical expression that closely approximates Baraff's curves. Their expression is often used to predict the ionization rates as a function of electric field for any operating temperature by using the expected temperature dependence of E_r and λ.

Crowell and Sze's expression was used to obtain an effective ionization rate for each of the six samples at various temperatures. At room temperature for example, E_i and E_r were set to 3/2 E_g = 2.2 eV and .022 eV, respectively, and λ was allowed to vary so as to satisfy the breakdown condition for each device. The effective ionization rate was then calculated as $\alpha_{eff} = 1/l_a$ where l_a was determined as $\int_0^{l_a}\alpha dx = .95$. Room temperature values of α_{eff} are plotted in Figure 19 as a function of electric field averaged over the ionization region (l_a). The slopes shown passing through the data were inferred from small-signal admittance data. An effective

ionization rate as a function of temperature was deduced from these data and expressed as

$$\alpha(E,T) = \alpha_{\infty}(T)\ \exp\{-(b(T)/E)^2\} \qquad (9)$$

where the ionization coefficients $\alpha_{\infty}(T)$ and $b(T)$ are listed in Table VI along with selected temperature dependent coefficients reported by others

Table VI

Temperature Dependent Ionization Coefficients

	$\alpha_{\infty}(T) = \alpha_{\infty}(T_0)[1 + a(T - T_0)]$		$b(T) = b(T_0)[1 + c(T - T_0)]$	
	$\alpha_{\infty}(T_0)$	a	$b(T_0)$	c
Hall and Leck	$2.00 \times 10^5\ cm^{-1}$	.07%/°C	5.00×10^5/V	.12%/°C
Wiesman, et al.	$1.60 \times 10^5\ cm^{-1}$	.17%/°C	5.55×10^5/V	.11%/°C
Expression 9	$1.47 \times 10^5\ cm^{-1}$	.07%/°C	5.55×10^5/V	.11%/°C

Another comparison of the inferred rates with low-field data recently published by Pearsall et al.[32] is also shown in Figure 19. The long-short dashed curves are the results of a linear regression analysis of their data between $2.3 \times 10^{-6} < 1/E < 3.2 \times 10^{-6}$, which gave

$$\alpha_n = 7.8 \times 10^5\ \exp\{-(8.0 \times 10^5/E)^2\}$$

$$\alpha_p = 1.6 \times 10^5\ \exp\{-(6.5 \times 10^5/E)^2\}.$$

The dotted curve is a weighted average of these values, i.e.,

$$\alpha = \frac{\alpha_n - \alpha_p}{\ln\alpha_n - \ln\alpha_p}\ , \text{ and}$$

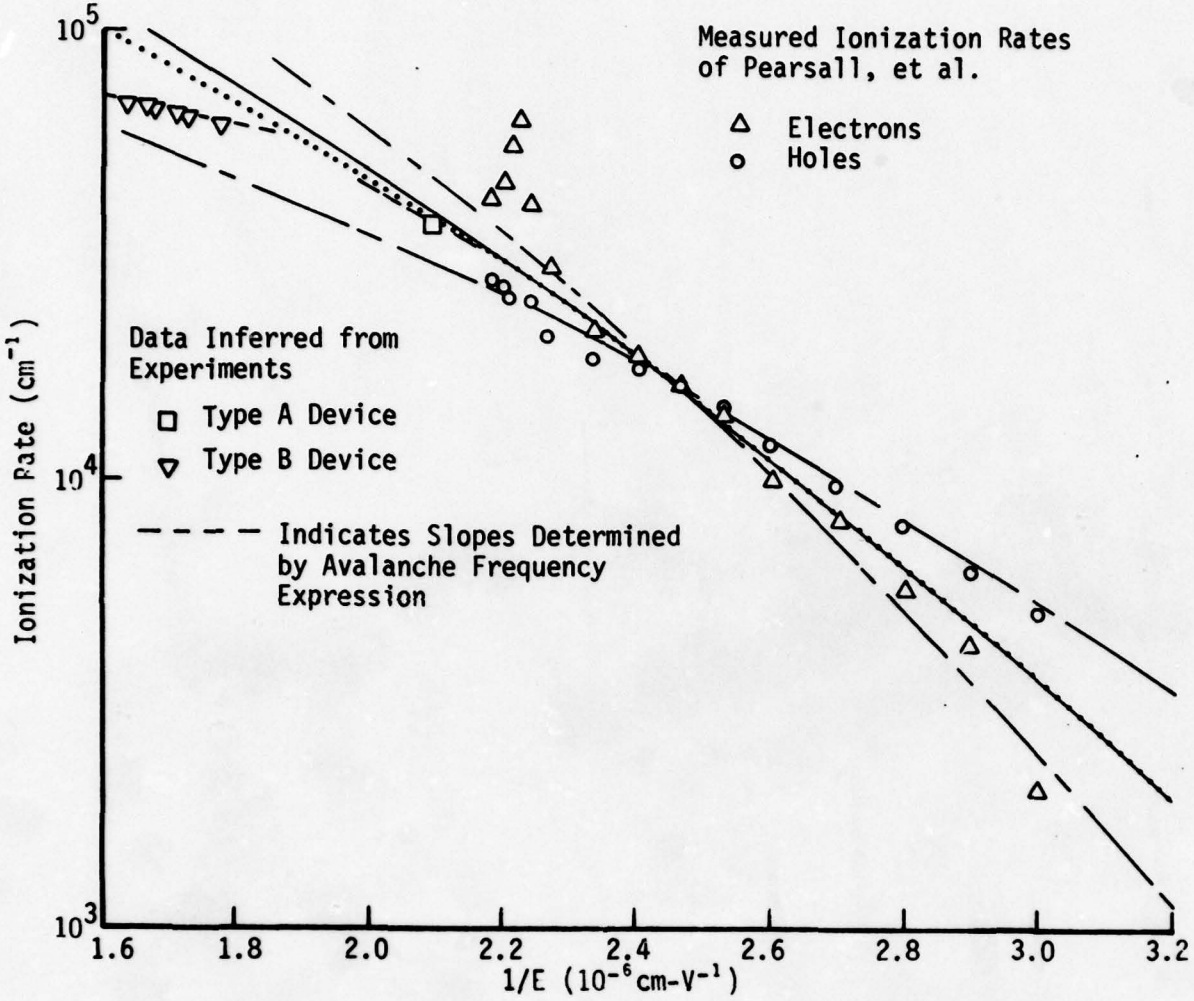


Figure 19. Inferred Ionization Coefficients Compared to Latest Low-Field Measurements.

the solid line was calculated from Crowell and Sze's[31] analytical approximation using E_r = 0.022 eV, E_i = 2.2 eV, and λ = 35Å.

Although results of d.c. calculations with the data of Pearsall et al. (extrapolated into the high-field region) gave reasonable agreement with measured values for device type A, the results for type B device differed significantly. Consistent results between breakdown calculations and measurements for both types were obtained only with the rates determined empirically. Table VII compares measured breakdown voltages and temperature coefficients of breakdown with those calculated with the inferred rates.

MICROWAVE CHARACTERISTICS

Based on the circuit model of Section III, microwave characteristics are determined by the drift width, l_d, the derivitive of the ionization coefficient with respect to the electric field, $\bar{\alpha}'$, the avalanche frequency, ω_a, the effective velocity, $\bar{v}$, the current multiplication factor, $\bar{M}$, and the space charge factor k_1. D.C. calculations indicate that the avalanche width, l_a, and the derivitive of the ionization rate, $\bar{\alpha}'$, changes little with temperature or bias current when the highly doped spike is within 3000Å of the junction. The drift width, l_d, however, changes significantly with both temperature and current for non-punch thru devices. The saturated drift velocity, $\bar{v}$, also changes significantly with temperature which, in turn, causes the avalanche frequency to be temperature dependent.

Breakdown calculations were made to estimate the drift width at various current levels. Figure 20 shows the calculated electric field profile of a type A device for two different bias condiditions. The depletion width is seen to increase from about 2.80 microns to 3.77 microns. Self-heating was included in these calculations assuming a thermal resistance of 14.5 °C/W.

TABLE VII

COMPARISON OF MEASURED AND CALCULATED VOLTAGES

USING INFERRED RATES

	DEVICE NUMBER					
	3	9	12	14	16	21
Measured V_B (volts)	27.8	42.3	36.3	42.1	35.2	31.9
Calculated V_B (volts)	28.6	40.9	36.4	40.1	36.6	33.4
Measured β ($\times 10^{-3}$/°C)*	3.2	2.4	2.7	2.6	3.1	2.8
Calculated β ($\times 10^{-3}$/°C)	3.1	2.2	2.7	2.5	2.9	2.7

* $\beta \triangleq \frac{1}{V(T_o)} \frac{\Delta V}{\Delta T}$

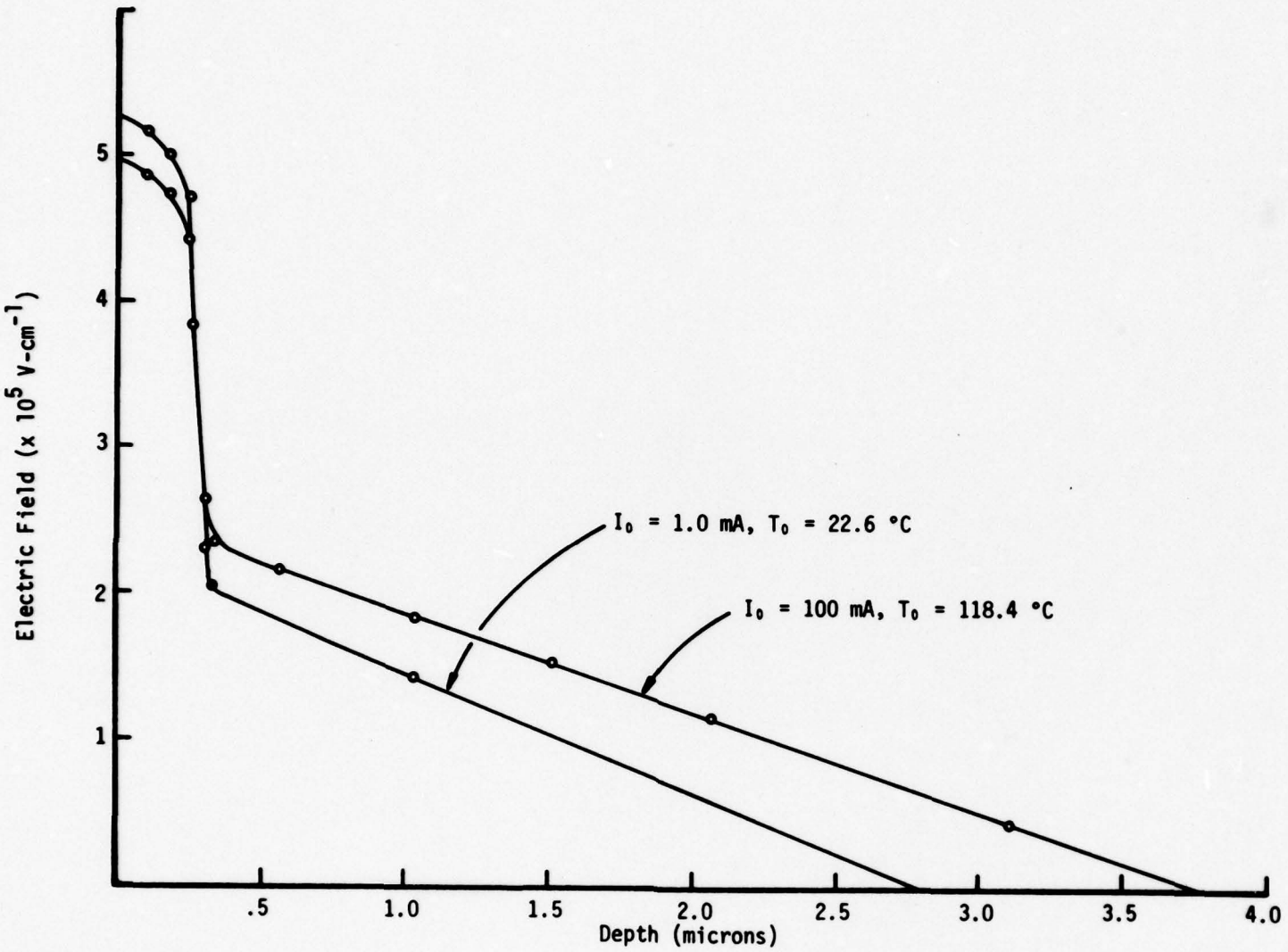


Figure 20. Electric Field Distribution for Type A Device.

The increase in depletion width with bias current, is also apparent in the low-frequency admittance data shown in Figure 21. These data were determined from a chip mounted in a standard microwave pill package. The impedance of the packaged device was first measured on an automatic network analyzer with d.c. bias current as a parameter. The data were then modified theoretically by extracting known test fixture parameters from the overall impedance data, thereby determining chip impedance.

After these measurements, the chip was removed from the package and its diameter determined by SEM techniques. The particular chip represented by the admittance data of Figure 21 showed a junction capacitance at breakdown of 0.81 pF and a diameter of 6.5 mils. These values imply a total depletion width of 2.8 microns at room temperature.

A series of admittance calculations were made using expression [8] for a range of device parameters. These were compared to experimental data in an attempt to determine more about the differential conductance term and the saturation current term. For convenience, these were combined into one term by defining $K \triangleq R_a C_a + G_a L_a$.

Figure 22 shows calculated curves for the device parameters listed in Table VIII. These gave a reasonable fit to the experimental data, especially about the origin of the admittance plot where the values of f_a and K had the greatest effect on the admittance curves.

The general trend of the K values were observed for a variety of device types. Efforts to relate them to physical phenomena or material parameters met with only limited success. For example, if the values of K were attributed only to positive differential conductance, they would imply a k_1 value of -17.0 at 50 mA. Since $|k_1|$ should be approximately 1.0, this interpretation

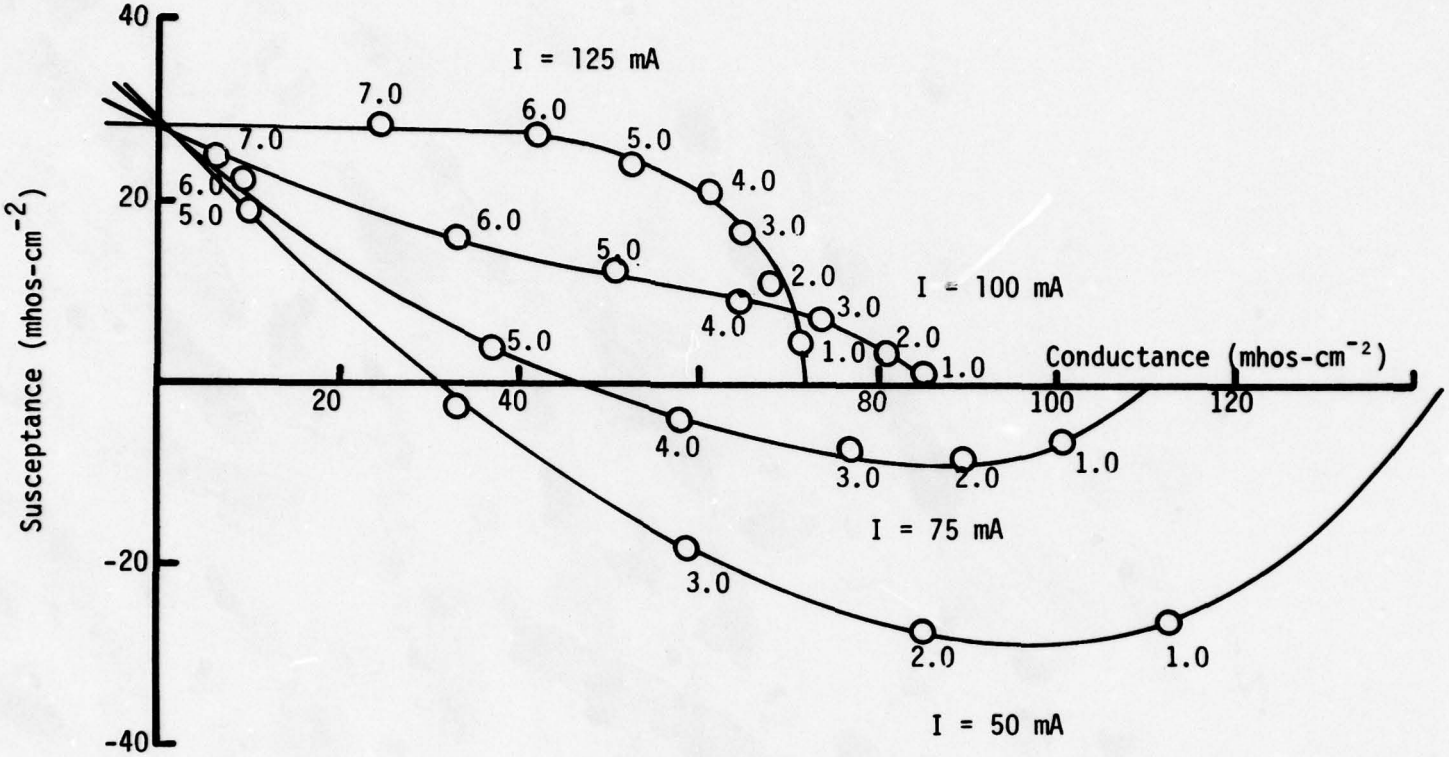


Figure 21. Measured Low-Frequency Admittance of Type A Device.

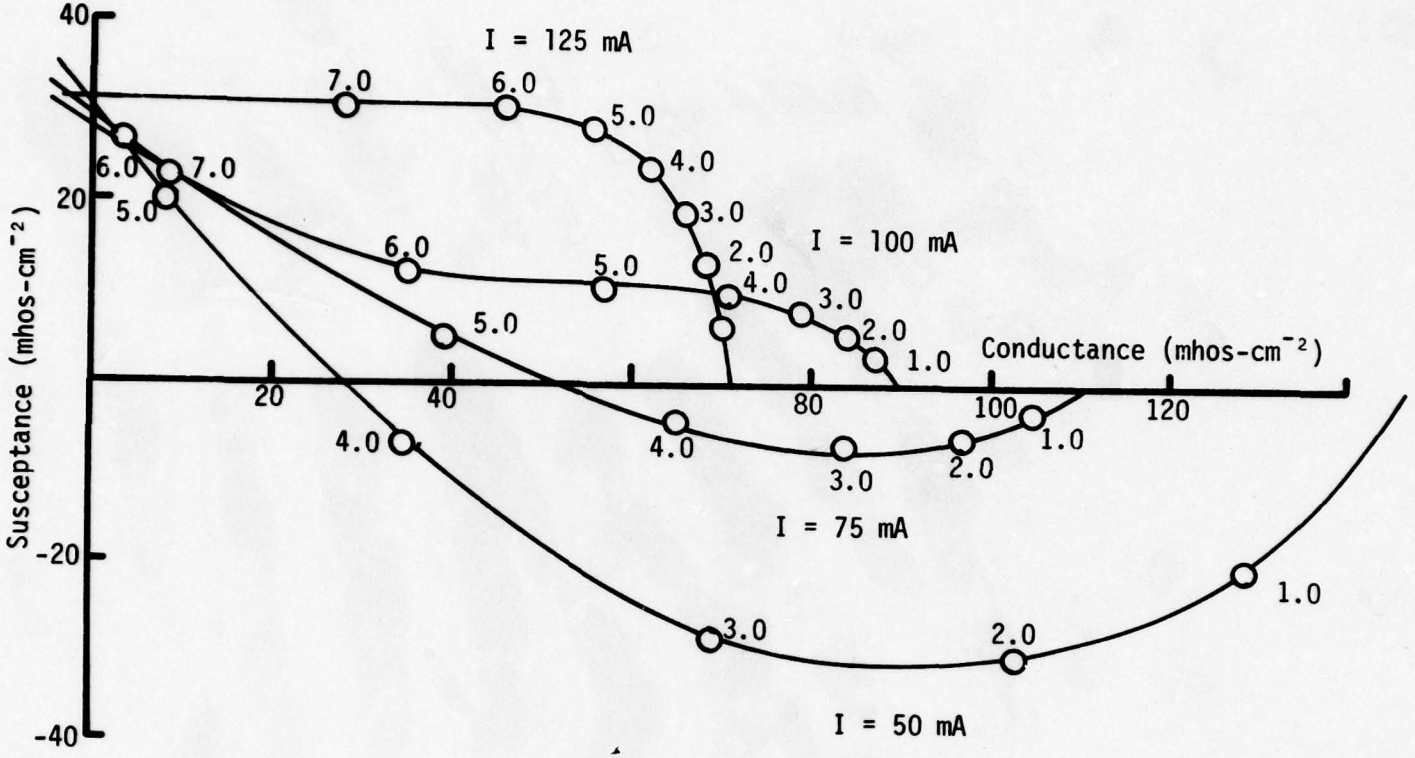


Figure 22. Calculated Low-Frequency Admittance of Type B Device.

Table VIII

Best Fit Diode Parameters

Determined From Breakdown Calculations					Determined by Curve Fitting Admittance Data					
I mA	T K	W μ	C_T pF	l_d μ	f_a GHz	l_d μ	K psec	$\bar{\alpha}'$ -	v^* 10^6 cm/sec	τd 10^{-12}
50	330	3.06	.75	2.81	4.7	2.60	6.0	.23	5.70	46.
75	348	3.25	.70	3.00	5.9	3.00	5.0	.25	5.45	55.
100	370	3.48	.65	3.23	6.4	3.30	4.0	.27	5.30	64.
125	396	3.77	.60	3.52	7.9	3.70	3.0	.30	4.95	75.

* The velocity of carriers were chosen to be in close agreement with that determined experimentally by Kramer[38] and Okamato and Ikeda[39]

seems unreasonable. If the values of K were attributed only to excess saturation current, they would imply avalanche multiplication factors which varied from 120 to 85 as the current increased from 50 to 125 mA. This interpretation is more consistent with the observation of others.[36] The type B devices, with the thinner avalanche regions, showed significantly higher K values. This suggests that the low multiplication factors may be due in part, to appreciable tunnel currents.[37] These effects are all temperature dependent and are difficult to characterize quantitatively.

Interpreting the experimental data in terms of a complex natural resonant frequency helped resolve severe stability problems encountered on an AFAL power combining program conducted here at Georgia Tech. Initial tests on series connected silicon chip devices were plagued with relaxation type oscillations at frequencies from about 1 GHz to about 4 GHz for low d.c. current levels. Although a single chip would operate well when biased to over 100 mA, a series pair would become unstable at current levels of 30-40 mA. Statistically, the data of these tests showed a "probable" linear relationship between the frequency of spurious oscillations and the square root of the current density at which instabilities occurred. This behavior tended to relate the instability of one chip to possible parametric effects associated with the avalanche resonance of another chip. This led to a working hypothesis that instabilities occurred in series connected devices when the avalanche processes of one chip, acting alone or with other circuit elements, provided a parallel resonance for the other chip(s) at or near a subharmonic of the operating frequency.

Other experiments were devised as further tests of this hypothesis. It was reasoned that, if the instability of one chip was caused by a resonance associated with the avalanche processes of another chip, it should be

possible to increase the current level at which breakup occurred by intentionally adding capacitance directly in parallel with each individual chip. By so doing, the troublesome resonance would be tuned to a lower frequency for a given d.c. current; the net result being that higher currents could be reached before the resulting resonance approached the same subharmonic at which instability occurred without the capacitors. The improved results obtained by adding parallel capacitance across each chip strongly supported the hypothesis that the instability was somehow related to the avalanche resonance since these experiments led to higher power series connected silicon devices.

Surprisingly, the first experiments with series connected high efficiency GaAs chips did not exhibit the same low-current instabilities that were consistently observed with silicon chips. This later proved to be the case with various other Schottky and p-n junction devices having both hi-lo and lo-hi-lo doping profiles. These results prompted further theoretical studies which dealt with basic device differences and their implication on circuit stability.

The manner in which the actual devices differ, especially about the "resonant" or avalanche frequency, is best illustrated by the small-signal admittance plots shown in Figures 23 and 24. These plots, obtained by reducing network analyzer data to chip admittance, are for c.w. silicon p^+-n-n^+ and GaAs Schottky lo-hi-lo devices. Also shown for the Si data are curves generated from the modified Read diode model whose parameters were chosen to obtain a "best fit" to the chip data for bias currents of 25 and 100 mA. The curves are based on the diode model in which the avalanche, or natural resonant, frequency is allowed to be complex (equivalent to

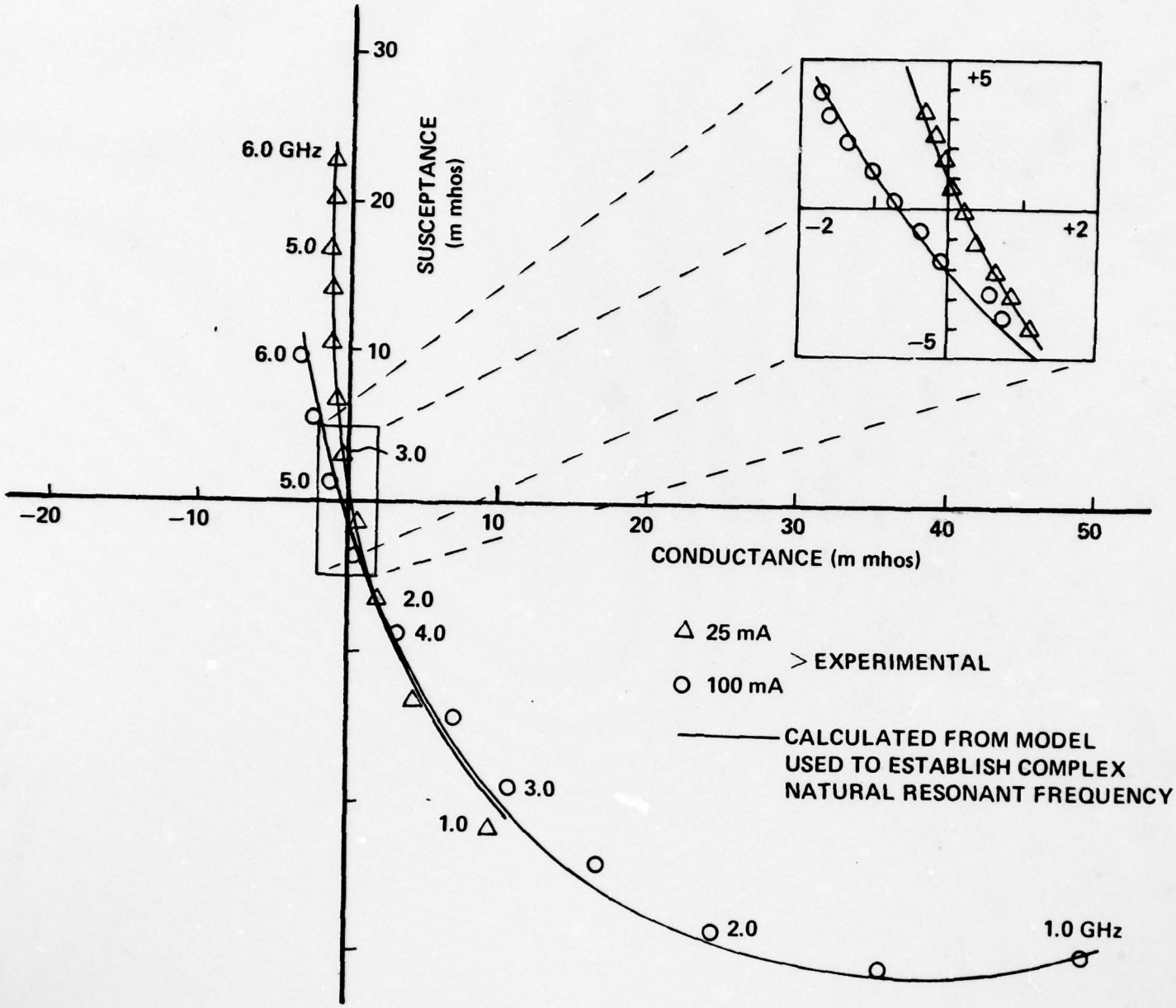


Figure 23. Small-Signal Admittance of Silicon p^+-n-n^+ Device.

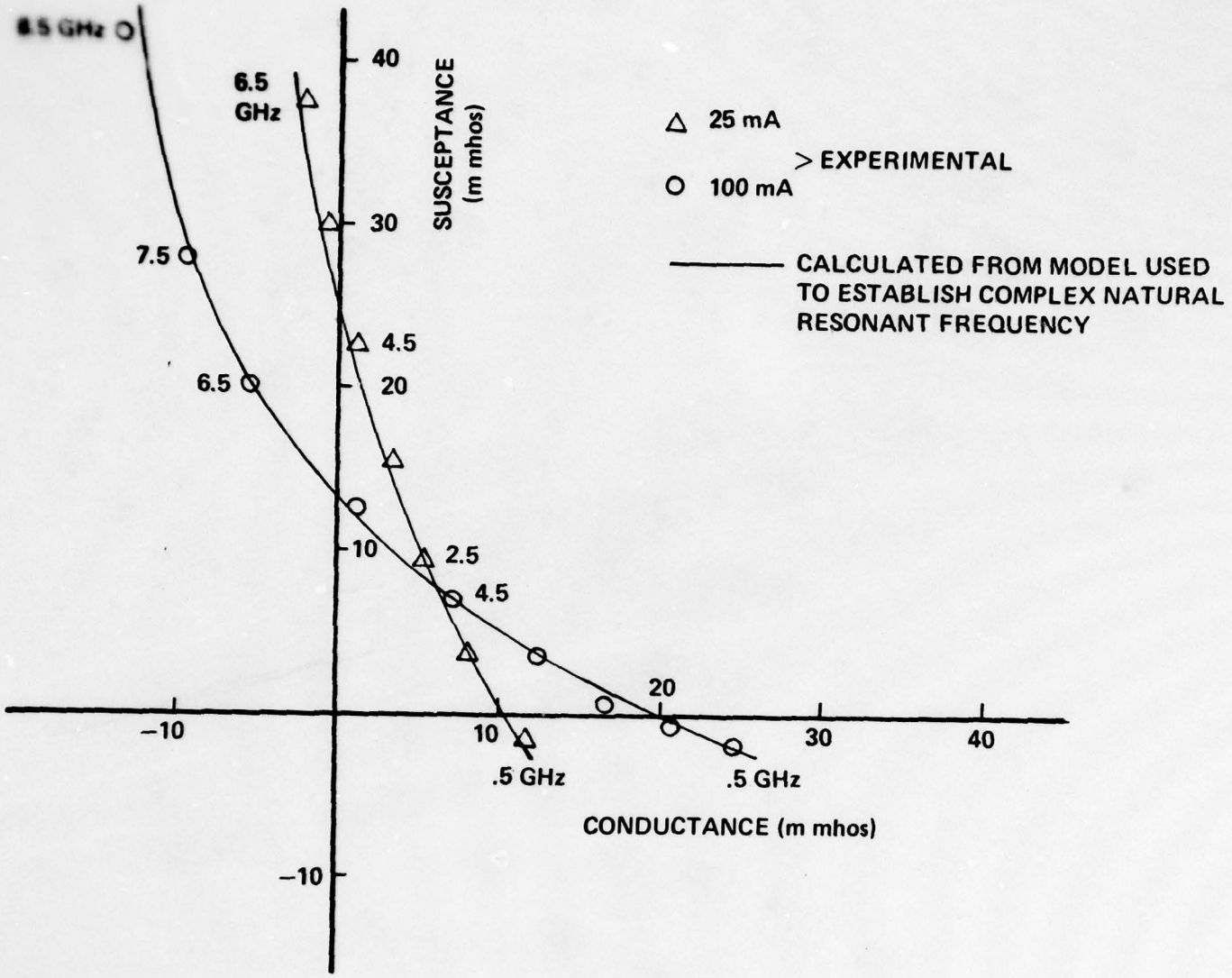


Figure 24. Small-Signal Admittance of GaAs lo-hi-lo Device.

including positive and negative resistive elements in the equivalent circuit of the avalanche zone as discussed previously).

Figure 25 is a plot of the complex natural resonant frequency (the pole, $s_a = \sigma_a + j\omega_a$, of the device impedance) obtained for each device by curve fitting the experimental data at the various d.c. bias currents. The real part of the complex frequency, σ_a, can be approximated by a negative term (corresponding to positive damping) which is independent of current and a positive term (corresponding to negative damping) which is directly proportional to bias current, i.e., $\sigma_a = k_1 + k_2 I_{dc}$ where k_1 and k_2 were chosen to fit the experimental data. The imaginary part is directly proportional to the square root of bias current and, of course, corresponds to the well known avalanche frequency.

The circuit model used to fit the data is identical to that described by Gummel and Scarfetter[20] who described the avalanche region of an IMPATT device by a complex function F, the poles of which correspond to its complex natural resonant frequency. The locus of the poles for their idealized diodes C1 and C5 are also shown in Figure 25. These poles were calculated assuming zero saturation current, hence they lie within the right half of the complex frequency plane (RHP). The effective avalanche widths of 1 and 5 microns, respectively, bracket the estimated value of 1.5 microns for the silicon chip used here.

The plots of Figure 25 are typical of a large number of devices measured. As seen, there is a significant difference between the complex natural resonant frequency (or pole in device impedance) of the silicon device and that of the GaAs device. The natural resonant frequency (hereafter referred to as pole) of the silicon chip enters the right half of the complex frequency

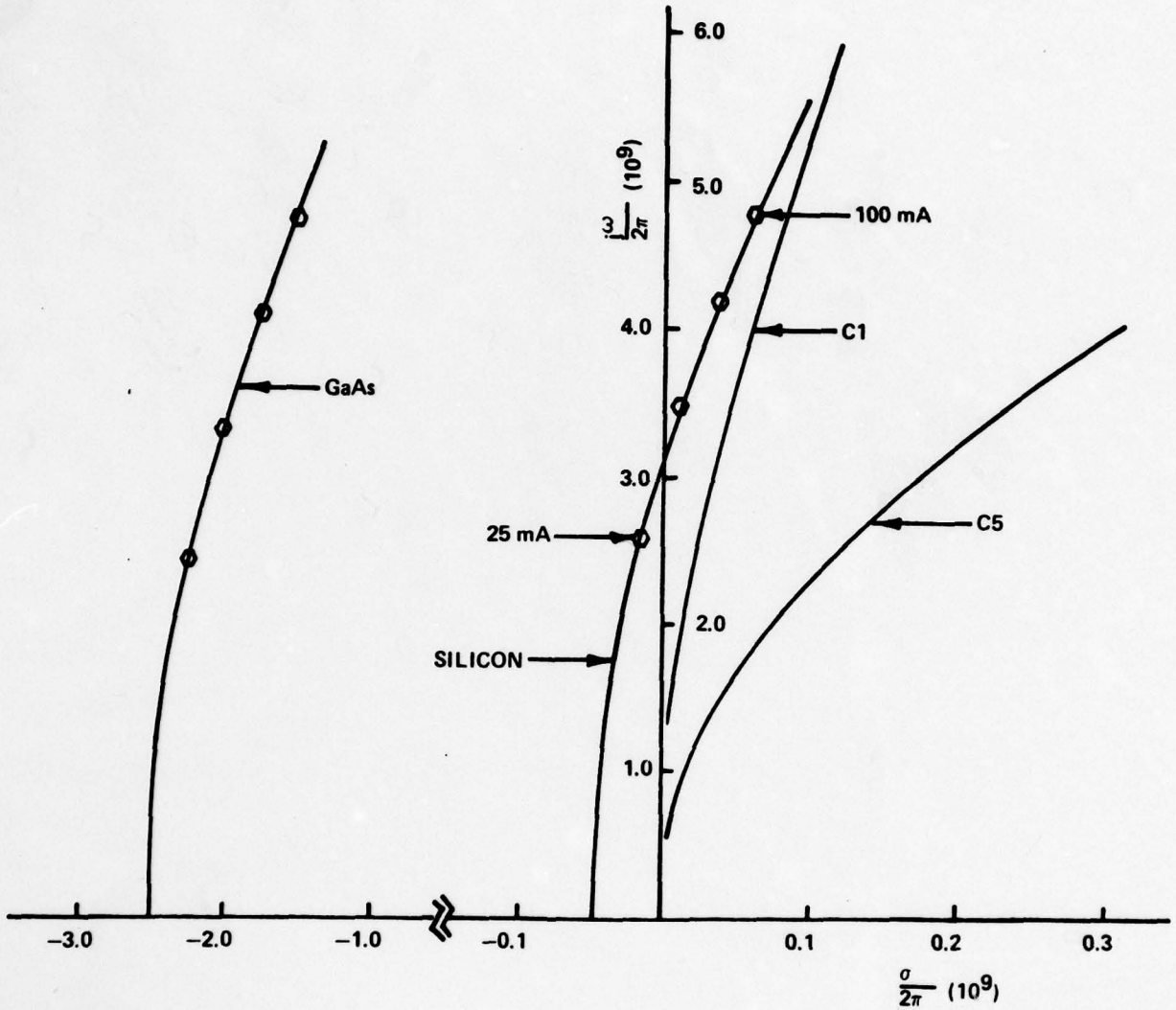


Figure 25. Locus of Natural Resonant Frequency for GaAs and Si Devices. Note scale change for GaAs device. (C1 and C5 after Gummel and Scarfetter[20]).

plane (RHP) for currents greater than about 30-40 mA. In contrast, the pole of the GaAs chip remains far from the RHP for all realistic currents. It is this difference that relates directly to the relative stability of the two devices.

For example, it is well known that when the zeros and poles of a two-terminal network lie in the RHP, then the network is short-circuited or open-circuited unstable, respectively. Consider the single chip circuit depicted in Figure 26a where the load impedance has been adjusted to give a zero in total impedance at the operating frequency ($s_0 = j\omega_0$) for a bias current of 50 mA. When the bias current is increased to 50 mA, the short-circuited network (shorted at the indicated terminals) would start oscillating at the frequency ω_0. The pole, which enters the RHP at a slightly lower current, would cause instabilities only if the network were open circuited (or nearly so) at the frequency ω_a. Normal IMPATT oscillator circuits and their associated bias arrangements offer sufficiently low circuit impedance to prevent this single chip instability at ω_a. On the other hand, consider the network depicted in Figure 26b, consisting of a load and two series connected chips. One chip now provides the open circuit for the other chip and visa versa, resulting in possible instabilities at ω_a under short circuited conditions. In fact, the series connection of two identical chips results in a multiple pole which becomes unstable at $s_a = j\omega_a$ or when s_a enters the RHP for both open and short circuited conditions.

Figure 27 shows the calculated pole-zero locus of a two chip network in which parallel capacitors are placed across each chip. The load impedance consists of a coaxial transformer and tuning inductor whose characteristics were adjusted to maintain a zero at $s_0 = j\omega_0$ for a bias current of 50 mA as capacitance was added in parallel to each chip. As clearly illus-

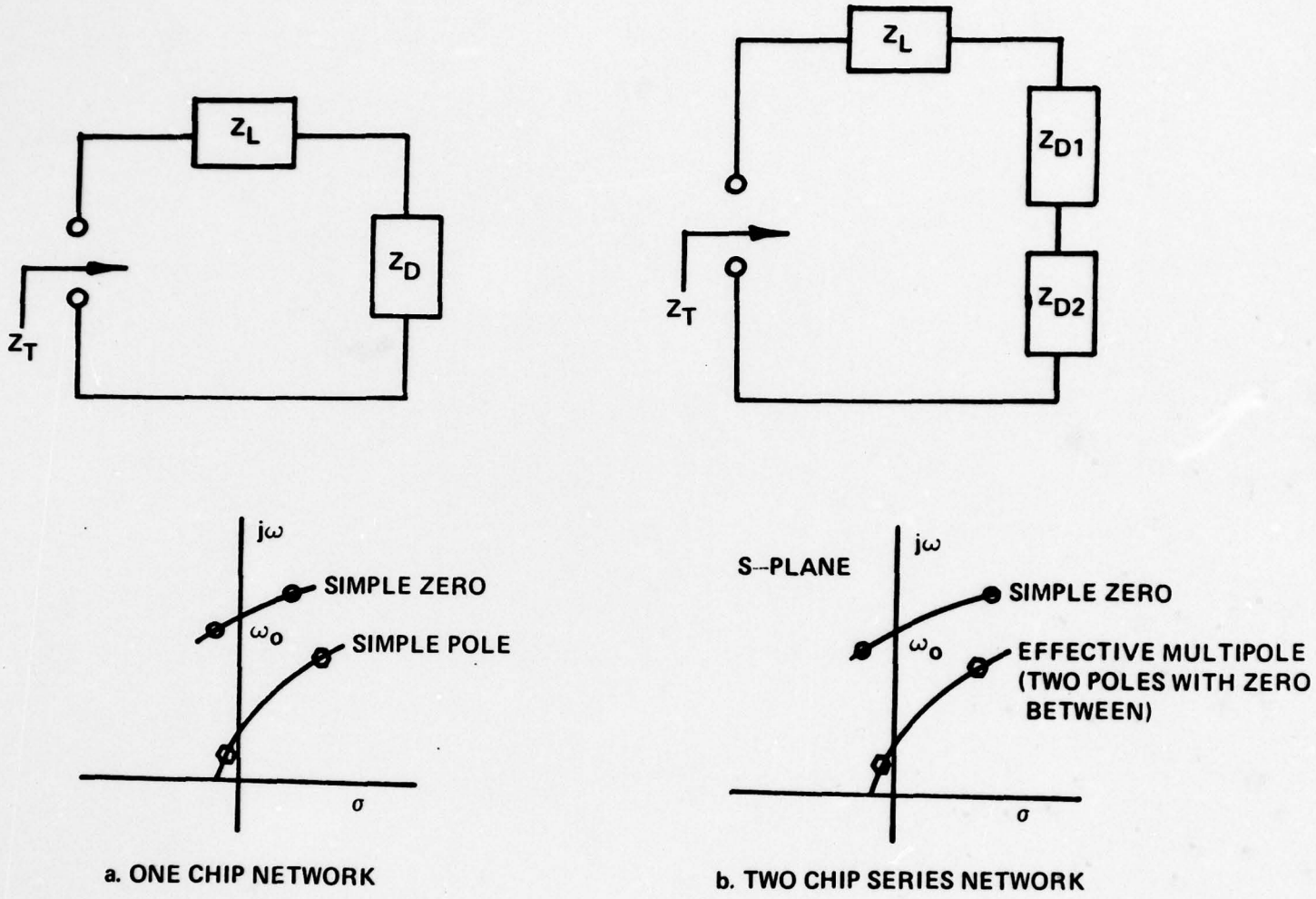


Figure 26. Oscillator Network Used to Illustrate Instability Problems of Series-Connected Chips.

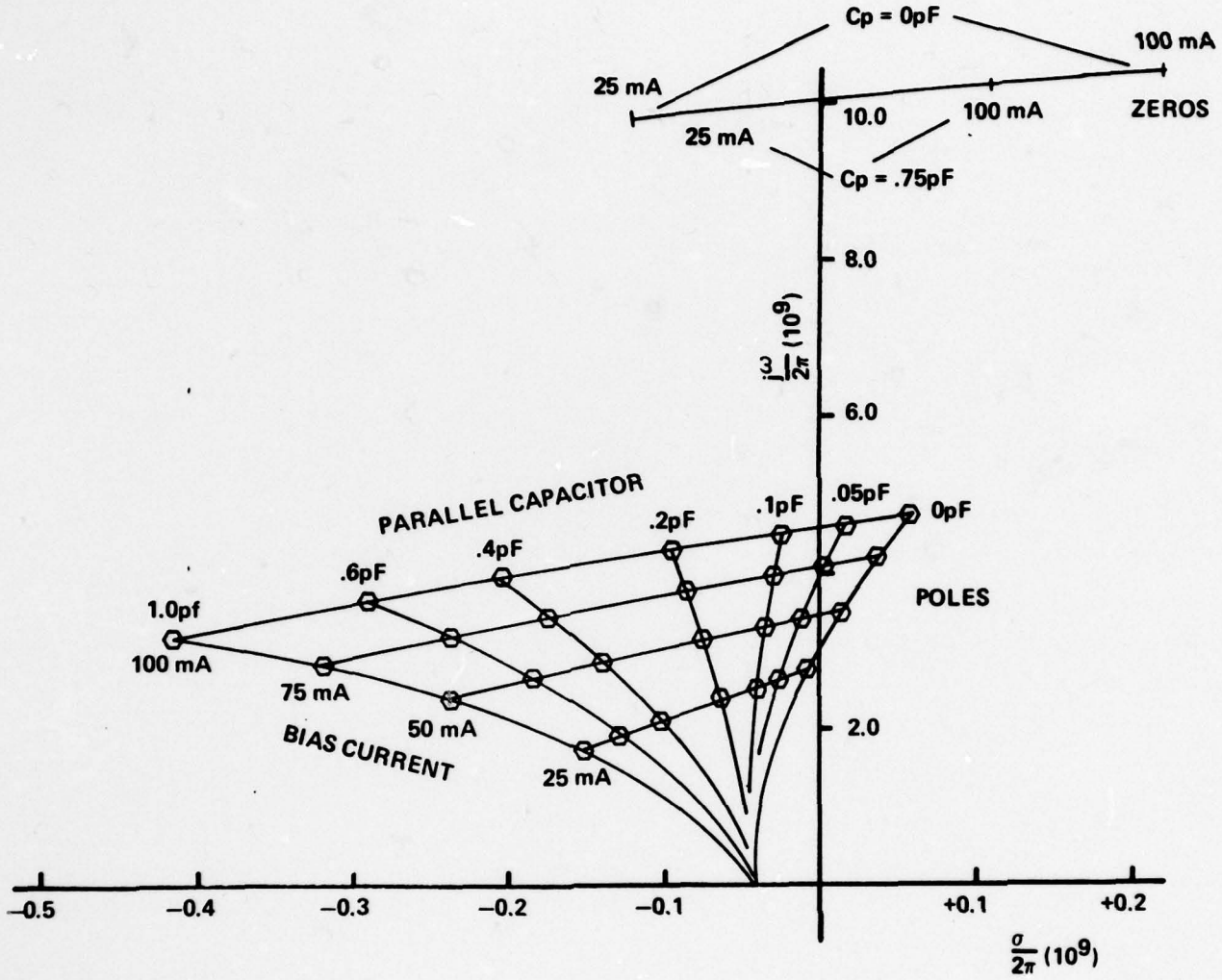


Figure 27. Effect of Parallel Capacitance on Locus of Poles of Network.

trated, the parallel capacitors shifts the locus of the poles, causing them to remain in the LHP and resulting in a stable network. These calculations are consistent with the following experimental observations.

1. series-connected silicon chips of the type used become unstable at bias current levels between 30 and 40 mA,

2. the instabilities occur at approximately one-third the operating frequency (initially thought to be parametric instabilities),

3. series-connected silicon chips remain stable up to burnout only with parallel capacitors,

4. series-connected GaAs chips of the types used are stable at current levels up to burnout.

Other calculations indicate that parallel capacitors across the individual chips greatly reduce the possibility of parametric type instabilities. Furthermore, bias circuit oscillations and related failures are considerably reduced and often eliminated entirely by use of the capacitors.

CONCLUSIONS

The breakdown calculations described in this section utilized the pseudolocal approximations of Okuto and Crowell[28] to determine a temperature dependent "effective" ionization rate from experimental data of selected lo-hi-lo devices. The rates thus obtained are in reasonable agreement with values extrapolated from the low-field measurements recently reported by Pearsall, et al.[32]

The effective ionization rates were used to calculate certain device parameters. Others were obtained by curve fitting experimental data. The latter required values of K which implied current multiplication factors on the order of 100 for devices with avalanche widths of about 2500 Å. For devices with thinner avalanche widths, the multiplication factors were considerably lower. This suggests the possibility of appreciable tunneling

currents. The temperature dependence of these effects could not be accurately modeled.

Interpreting the experimental data in terms of a complex natural resonant frequency helped resolve the cause of severe stability problems encountered on a chip level power combining program conducted concurrently here at Georgia Tech.

SECTION V

PUBLICATIONS AND PRESENTATIONS

The results of this work were presented in the following publications:

"Microwave Lumped-Element VCO and Multichip Power Combiners," Eleventh Annual Asilomar Conference on Circuits, Systems and Computers, Conference Record, pp. 173-179, November 1977, (partially supported by ARO).

"Transient Temperature Profiles Within the Active Region of Uniformly Doped and High-Low Doped Schottky IMPATT's," IEEE Trans. on Electron Devices, Vol. ED-25, No. 9, pp. 1160-1166, September 1978 (fully supported by ARO).

Another paper, partially supported by ARO, entitled "Multichip IMPATT Power Combining, A Summary with New Analytical and Experimental Results" has been accepted for publication in the December 1979 issue of the IEEE Trans. on Microwave Theory and Techniques.

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APPENDIX A

Description of MITAS II

The MITAS II program proved capable of performing detailed analyses of the heat flow, both transient and steady state, in complex semiconductor devices. This program was developed by Martin Marietta, Denver Division and evolved from a program entitled CINDA-3G, developed by Chrysler Corporation Space Division at NASA's Michoud Assembly Facility.

It consists of a FORTRAN preprocessor, which converts the user-supplied data into FORTRAN routines and block data. These routines contain the appropriate calls to the MITAS library. This extra compilation enables the user to write routines to change parameters and to assist him in generating input data where many points are involved. MITAS consists of a main program and over 280 subroutines and functions.

This section contains a brief description of the operation of MITAS II. The program is based on a model, or lumped parameter, representation of a physical device. A critical aspect of this approach is determining the optimum spacing between model points. In a transient analysis, time is "lumped" as well as space and careful consideration must be given regarding the tradeoffs in round-off error, economy, and stability. An example of a test calculation used to test the proper operation of MITAS is described at the end of this section.

The fundamental equation on which the model representation is based can be derived by writing an energy balance for an elemental volume of the body:

heat flowing in - heat flowing out + heat generated by internal sources = change in internal energy (1)

If the elemental volume is a rectangular prism with edges dx, dy, and dz, the energy balance given above may be expressed as

$$\frac{\partial}{\partial x}(k\frac{\partial T}{\partial x}) + \frac{\partial}{\partial y}(k\frac{\partial T}{\partial y}) + \frac{\partial}{\partial z}(k\frac{\partial T}{\partial z}) + Q_g = c\rho\frac{\partial T}{\partial t} \qquad (2)$$

where k = thermal conductivity of the material

T = temperature,

t = time,

Q_g = heat generated internally,

c = specific heat, and

ρ = density.

If k and Q_g are constant and the device is operating under steady state conditions, Eq. 2 reduces to either the Poisson equation ($Q_g \neq 0$) or the Laplace equation ($Q_g = 0$). Transient analyses must generally include both the spatial and time dependences shown in Eq. 2 .

The solution in the general case is further complicated when spatial uniformity and temperature independence cannot be assumed for the thermal conductivity k and the heat generated term Q_g. Such assumptions are often invalid for many microwave devices. The composite device structure is layered with metallizations of different thicknesses, different cross-sectional areas, and dissimilar materials. Furthermore, it is not uncommon for the operating conditions to introduce thermal excursions of 200 °C. Thermal conductivities of semiconductor materials are particularly sensitive to temperature fluctuations of this magnitude.

The development of an equivalent thermal circuit for the device and its associated heat sink forms a convenient vehicle for cataloging the

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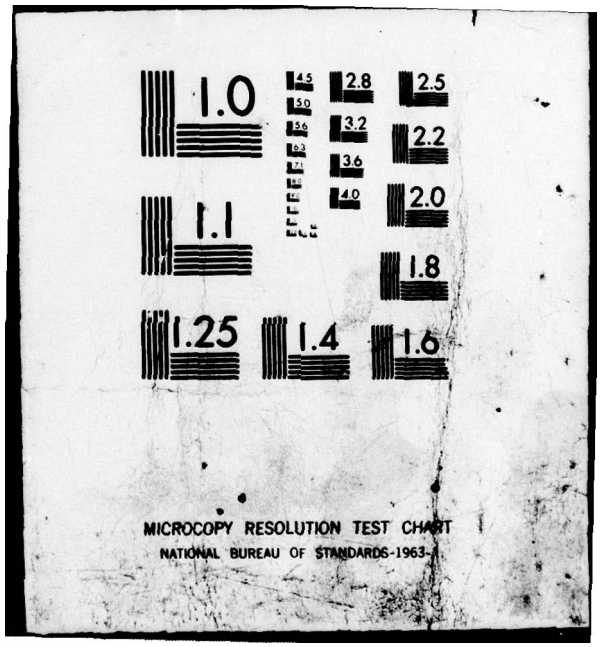
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equations that are developed when finite-difference techniques are applied to Eq. 2. A section of such an equivalent circuit is shown in Figure 1. The mass of the device has been subdivided into a mesh of nodes interconnected by heat conduction paths. The rate of heat flow Q_{ij} between node point $\underline{i}$ at temperature T_i and node point $\underline{j}$ at temperature T_j is written as

$$Q_{ij} = G_{ij} (T_i - T_j) \tag{3}$$

for conductive and convective heat flow and

$$Q_{ij} = G_{ij} (T_i^4 - T_j^4) \tag{4}$$

for radiative heat flow. Thermal conductance $\underline{G_{ij}}$ for a given path depends upon the heat transfer mechanism involved. Examples are presented below for conductive, convective and radiative heat transfer:

$$\underline{\text{conductive}}^* \qquad G_{ij} = \frac{kA}{\ell} \tag{5}$$

$$\underline{\text{convection}} \qquad G_{ij} = hA \tag{6}$$

$$\underline{\text{radiation}} \qquad G_{ij} = \sigma F_{ij} A_i \tag{7}$$

*Conductive heat transfer is by far the most important in IMPATT devices. The latter two are given for completness.

where A = cross-sectional area

ℓ = path length

h = convective heat transfer coefficient

σ = Stefan-Boltzmann constant

F_{ij} = geometric shape and emissivity factor for grey body radiators

A_i = surface area

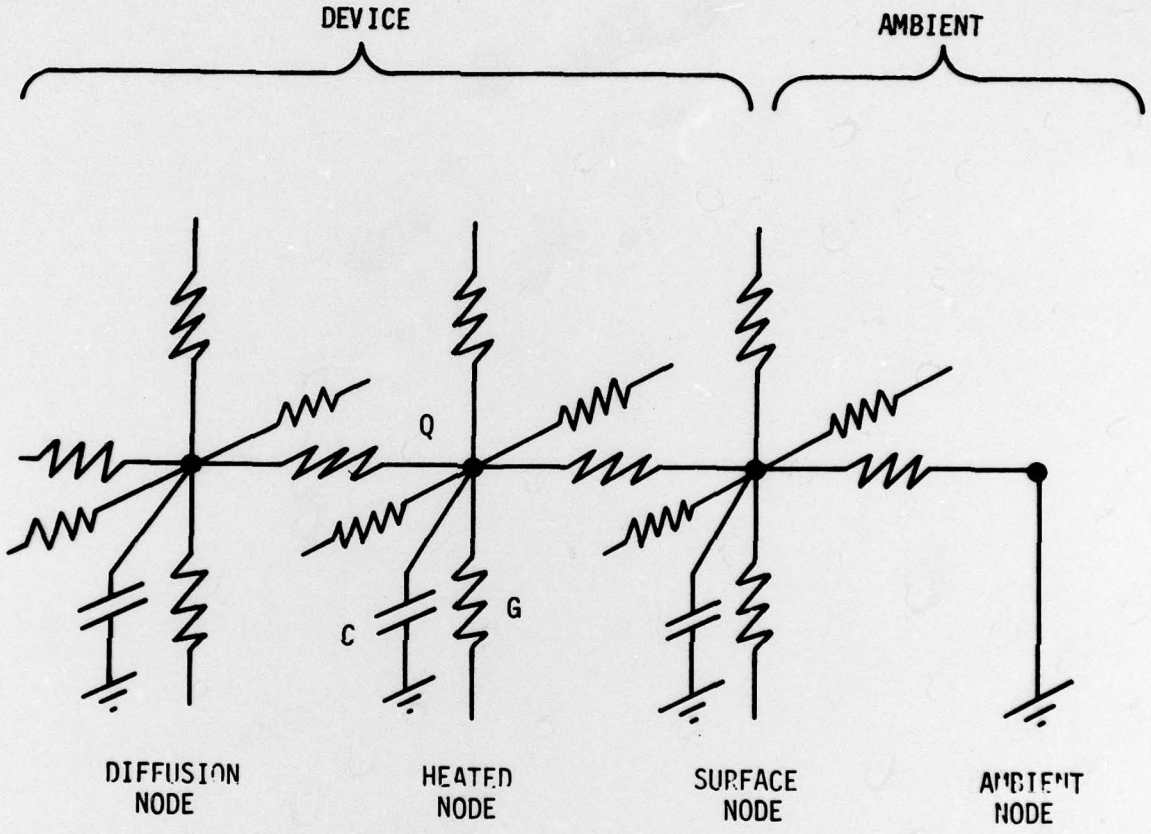


Figure A-1. Nodal Network Representation for Transient Thermal Analysis Illustrating the Heat Transfer Mechanisms.

As indicated in Eq. 2, the elemental mass associated here with a node point will experience a change in internal energy during transient conditions. This energy storage is mathematically described for the nodal model as

$$m_i c_i \frac{\partial T_i}{\partial t}$$

where the product $m_i c_i$ is defined as the thermal capacitance $\underline{C_i}$ of node $\underline{i}$.

A forward-difference representation of Eq. 2 for an interior node of the network shown in Figure 8 is written as

$$\sum_{j=1}^{m} G_{ji}(T_j - T_i) + Q_i = C_i\left(\frac{T_i' - T_i}{\Delta t}\right) \tag{8}$$

where $\sum_{j=1}^{m}$ = net influx of heat to node i via non radiative paths

Q_i = source or sink for node i

T_i = temperature at time t

T_i' = temperature at time $t + \Delta t$.

An additional term of the form

$$\sum_{j=n}^{v} G_{ji}(T_j^4 - T_i^4)$$

would be included on the left side of Eq. 8 for surface nodes capable of radiating to ambient sinks. Temperature variations of $\underline{k}$ and $\underline{c}$ are incorporated into the numerical solution by performing a table look-up at the start of each time step iteration. The "future" value of temperature is found by solving Eq. 8 for T_i', that is

$$T_i' = T_i + \frac{\Delta t}{C_i}\left(Q_i + \sum_{j=1}^{m} G_{ji}(T_j - T_i)\right) \tag{9}$$

It is important to observe stability requirements in numerical solutions of partial differential equations. Thermodynamic considerations for conduction heat transfer require a positive coefficient for the "present" temperature T_i given in Eq. 9. This condition is mathematically expressed as

$$\frac{\Delta t}{C_i} \sum_{j=1}^{m} G_{ji}(T_j - T_i) \leq 1 \tag{10}$$

If the length $\underline{\ell}$ (contained in the definition of G_{ji}) and the time step Δt are selected to satisfy Eq. 10, then a stable solution can be obtained.

The MITAS II program contains various solution methods based on the thermal analog model presented in Figure A-1.

The user must, therefore, model his device by dividing the space to be investigated into incremental volume elements (nodes). There are three types of nodes; diffusion nodes, arithmetic nodes, and boundary nodes. Each diffusion node is assigned a capacitance, which is the mass of the incremental volume times the heat capacity of the material. Heat capacity may vary with temperature. Arithmetic nodes have no mass. Therefore, they have no ability to absorb heat, and are used primarily for the user's convenience. Boundary nodes, as the name implies maintain a constant temperature, specified by the user. Each node is assigned an initial temperature and heat input. Heat input can remain constant or vary with temperature and/or time.

The network is completed by connecting the nodes with conductors, which represent thermal conductivities between the various points in space.

The conductances (i.e., thermal conductivities) can be constant or can be made to vary as the material(s) change temperature. The program is designed to handle up to 8191 nodes and 12287 distinct conductors.

Transient solutions are achieved by interative calculations of heat flow and temperature rise of nodes during a user-specified time step. The user specifies the maximum temperature change between iterations. When this criterion is satisfied, the program goes to the next time step. The steady state solutions are numerical solutions of Poisson's equation, with energy balance as the convergence criterion.

MITAS II uses a block format for inputting data and instructions. Briefly these consist of:

Input Options Block. This block inputs options to store, recall, update, or change complete problems.

Title Block. This block notifies the preprocessor of the type problem to be performed and provides information for title printout.

Node Data Block. This block contains data for each node consisting of node number, initial temperature, and capacitance value.

Conductor Data Block. This block contains data for each conductor consisting of conductor number, adjacent node numbers, and conductance values.

Constants Data Block. This block contains constants concerning maximum number of iterations, maximum temperature change allowed per iteration, time step, etc.

Array Data Block. This block contains the look-up tables describing the temperature dependence of k and c.

Program Controls Blocks. These blocks contain instructions and operations to be performed prior to, during, and after execution.

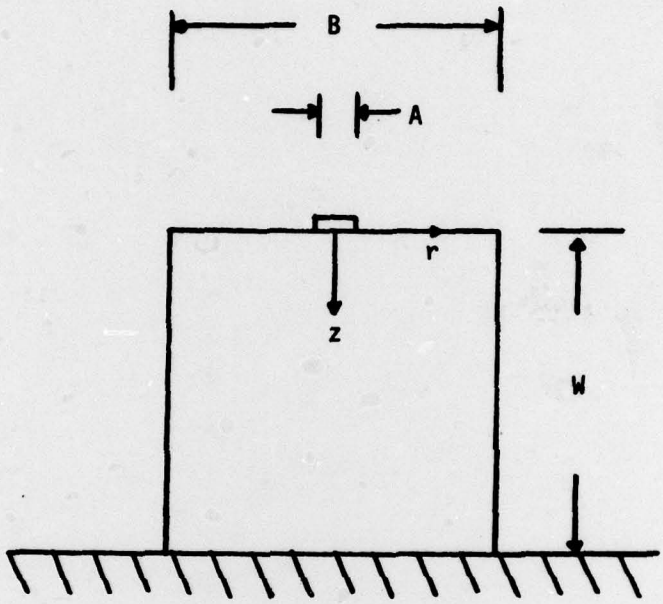
In adapting MITAS to the study of solid state devices, three of the problems which were encountered were (1) how to best model problems which are most easily described by cylindrical coordinates, (2) how to take advantage of symmetry to reduce the number of nodes and conductors, and (3) how to change scale so that a region having high temperature gradients has nodes which are spaced closely enough together.

In general, single mesa devices have been modeled by having nodes represent sectors of concentric cylinders. Thus, both capacitance and conductance vary with mean cylindrical radius. This is especially convenient for axially symmetric devices, wherein the entire model consists of a wedge, which effectively reduces the problem to a two dimensional problem. Scale changes are quite straightforward so long as there are equal numbers of nodes in adjacent vertical sectors. Even this restriction is not necessary if one calculates the conductances between nodes which are not directly above and below each other. The annular ring devices also possess cylindrical symmetry and were modeled in a similar manner.

Several computer programs were written for generating the node and conductor data for different device geometries. The most widely used were based either on parallelepipeds or on sectors of cylindrical cylinders. These were called GDATAR and GDATAC, respectively. Input data asked for by these programs included maximum number of points in any layer, number of layers of this material, thickness of layers in microns, number of nodal points, material of layer, thickness of adjacent layer, number of nodal points in adjacent layer, material adjacent layers, etc. The output of the program are files containing all data required in the Node Data and Conductor Data Blocks.

A number of test calculations were made initially to verify operation of the MITAS II program and to gain familiarity with input constraints required to obtain a desired degree of accuracy. These first test calculations used a device model analyzed by Kennedy, who obtained analytical expressions for the temperature distribution within homogeneous solid cylinders. The case considered assumed uniform heat flux to enter a portion of one end of a cylinder with the other end maintained at constant temperature. Dimensions of the heat flux source and the cylinder were chosen to approximate a typical X-band IMPATT chip mounted on a copper post. Figure 2 shows the geometry of the test model and the analytical expression for the temperature distribution. A computer program was written for evaluating the temperature distribution of a model whose dimensions correspond to Kennedy's Case I. Points were taken from these curves and compared to those of the MITAS II computer program. Figures 3 and 4 show how the MITAS transient solution converge to Kennedy's well known steady-state solution as time increases.

Test Model: Steady State Solution Known Exactly



$$\frac{T_I(r;z)}{T_I(0;0)} = \frac{A^2/B^2(1 - \frac{z}{W}) + \frac{2A}{W}\sum_{\ell=1}^{\infty}[\sinh(\frac{\alpha_\ell}{B}(W - z))/\cosh\frac{\alpha_\ell W}{B}][J_1(\alpha_\ell\frac{A}{B})J_0(\alpha_\ell\frac{r}{B})/\alpha_\ell^2 J_0^2(\alpha_\ell)]}{\frac{A^2}{B^2} + \frac{2A}{W}\sum_{\ell=1}^{\infty}[J_1(\alpha_\ell\frac{A}{B})/\alpha_\ell^2 J_0^2(\alpha_\ell)]\tanh(\frac{\alpha_\ell W}{B})}$$

α_ℓ is the ℓth root of $J_1(x)[J_1(\alpha_k)] = 0$

Figure A-2. Steady State Analytical Solution from: D. P. Kennedy, "Spreading Resistance in Cylindrical Semiconductor Devices," JAP, Vol. 31, No. 8, August 1960.

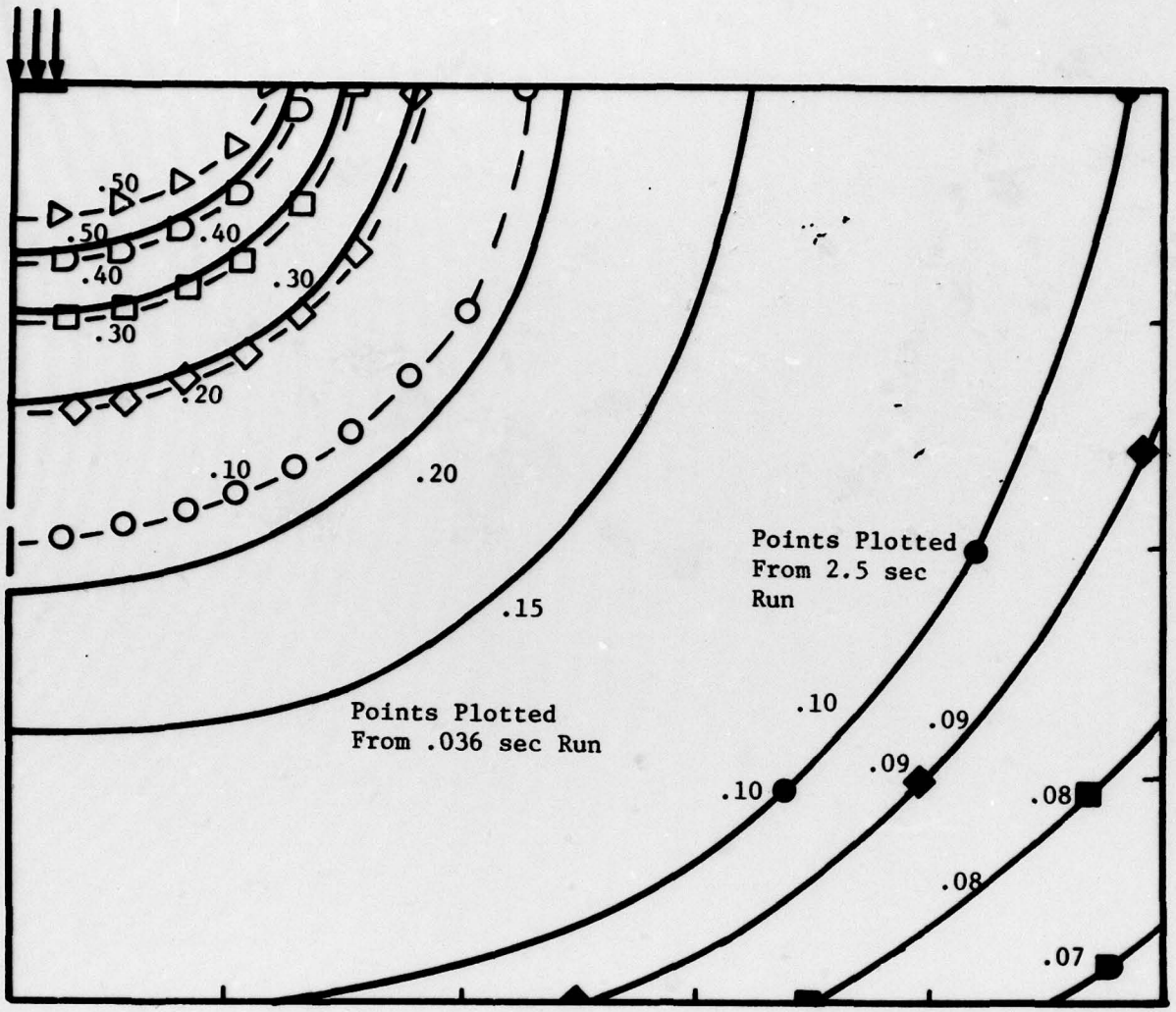


Figure A-3. Curves Illustrating Convergence of MITAS Transient Solution to Kennedy's Steady-State Solution (——Normalized isothermals from Kennedy's solution. Data points are corresponding transient isothermals for step application of flux).

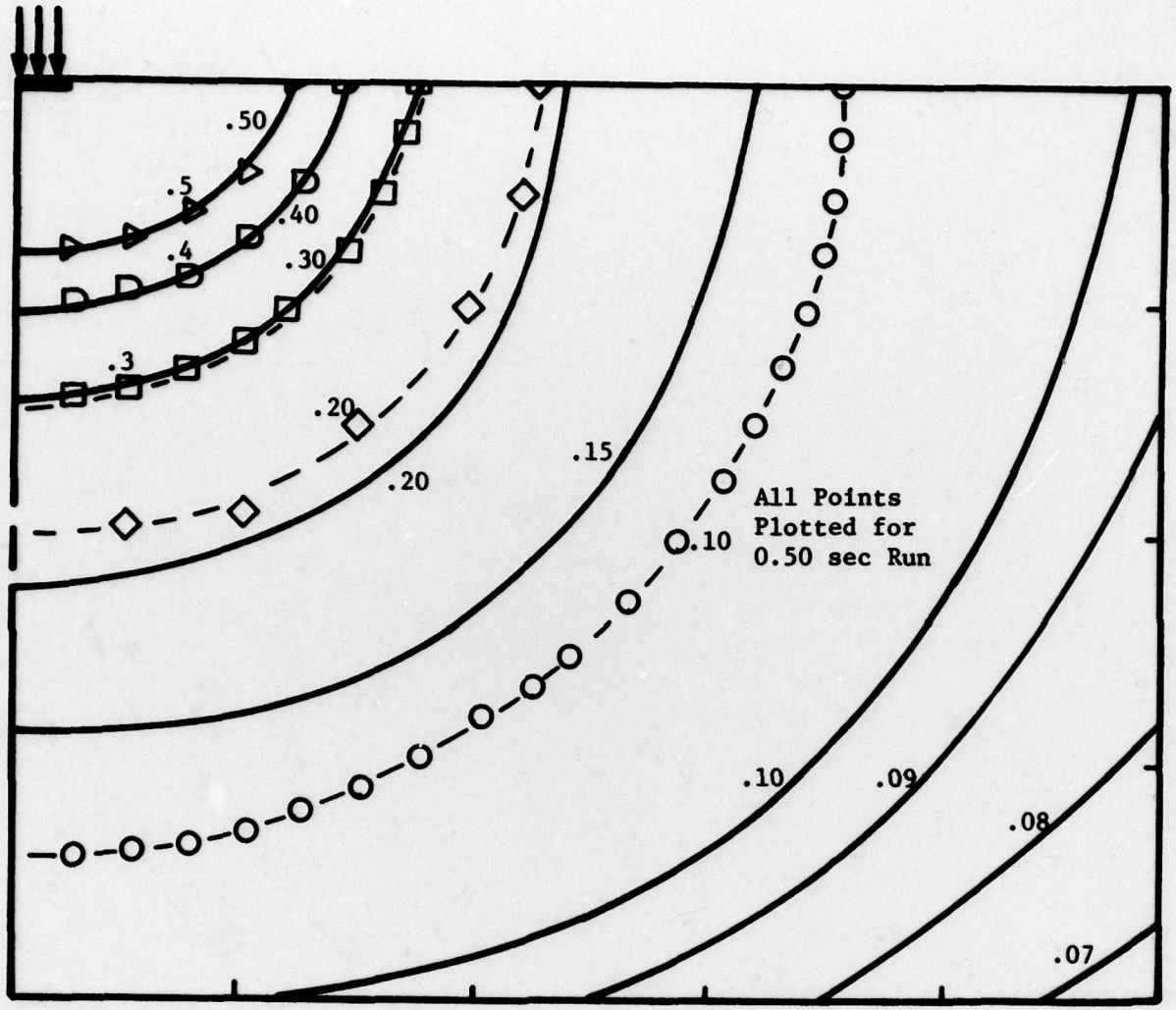


Figure A-4. Curves Illustrating Convergence of MITAS Transient Solution to Kennedy's Steady-State Solution (———Normalized isothermals from Kennedy's solution Data points are corresponding transient isothermals for step application of flux).